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Energy research Centre of the Netherlands

Crystalline Si Photovoltaics

Arthur Weeber

www.ecn.nl

Outline

- Short introduction ECN
- Introduction ECN Solar Energy
- General Si solar cells
- Crystalline Si Photovoltaics
  - Feedstock
  - Wafering
  - Cell processing
  - Module technology
  - Costs and environmental
- Summary

Petten: ECN; NRG; JRC; Covidien

Targets ECN research

Transition to renewable energy supply:

efficiency improvement

development of renewable energy

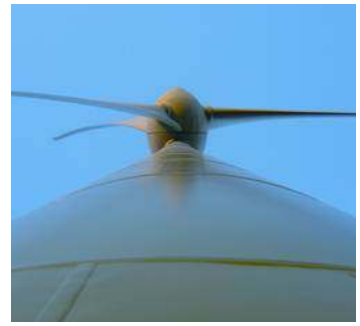
clean use of fossil fuels

maximum reliability
minimum environmental burden
optimal cost effectiveness

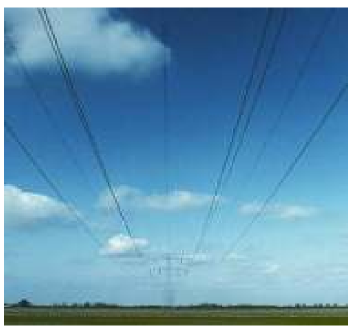
ECN Programme units + Contribution

Solar Energy
(21%)

Biomass, Coal & Environmental Research **(21%)**



Wind Energy
(11%)



Efficiency & Infrastructure
(17%)

Policy Studies
(11%)

H_2 & Clean Fossil Fuels
(19%)

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ECN Solar Energy

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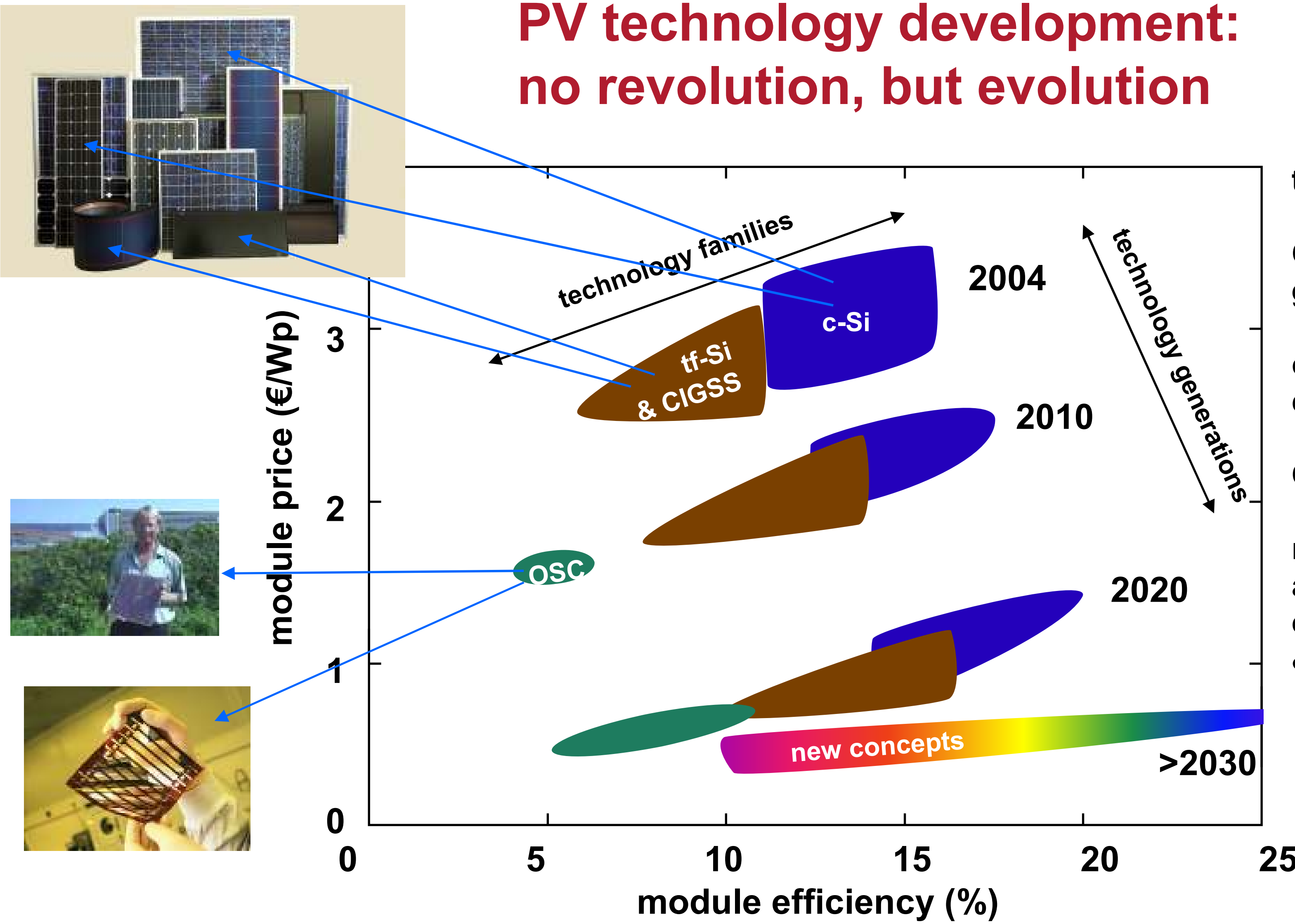
Solar Energy

- Silicon Photovoltaics
- Thin-Film Photovoltaics
- PV Module Technology

Objective:

- Price of solar electricity in 2015 the same as consumer electricity price, and after that even lower
  - High efficiency
  - Reduction of material use
  - Cost effective and environmental friendly processes and products
  - Long lifetime of the modules

PV technology development: no revolution, but evolution



tf-Si = thin-film silicon

CIGSS = copper-indium/gallium-selenium/sulfur

c-Si = wafer-type crystalline silicon

OSC = organic solar cells

new concepts = advanced versions of existing technologies & new conversion principles

(free after W. Hoffmann)

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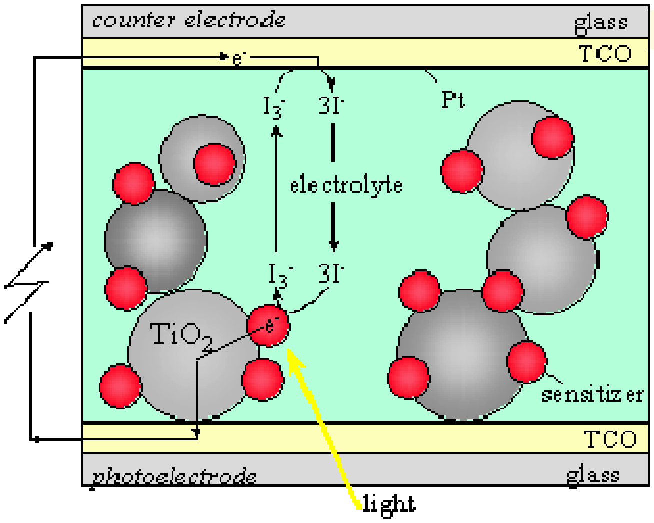
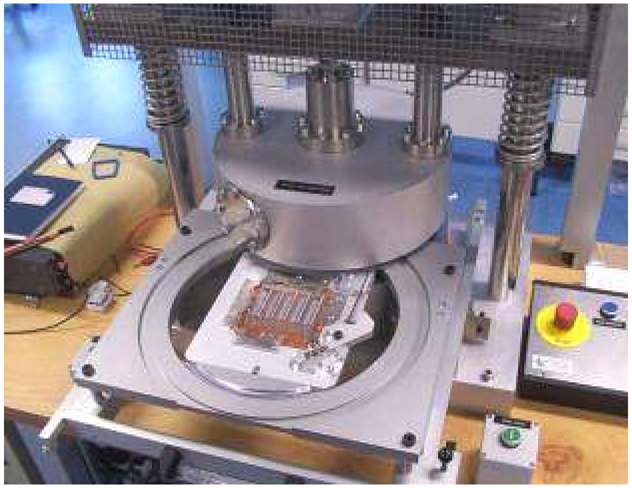
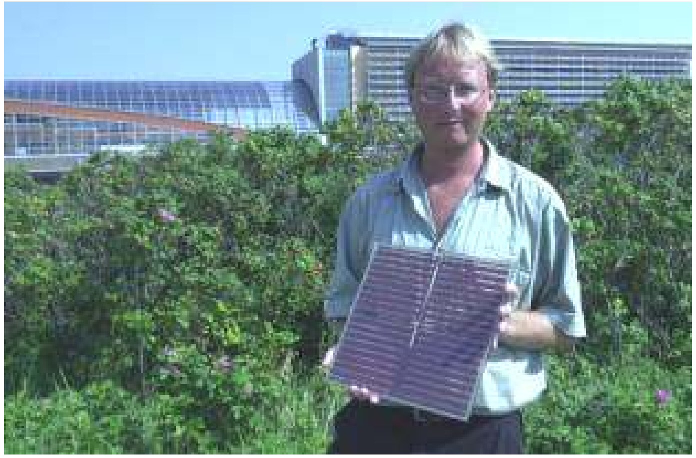
Thin-film photovoltaics

- Sensitised oxides







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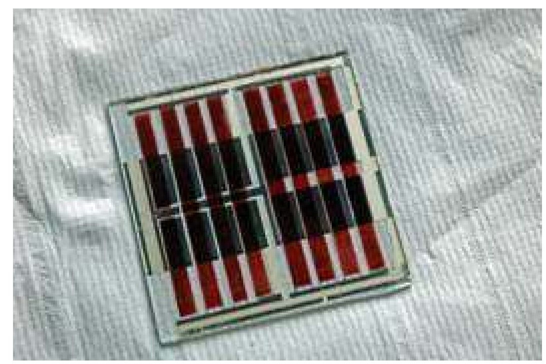
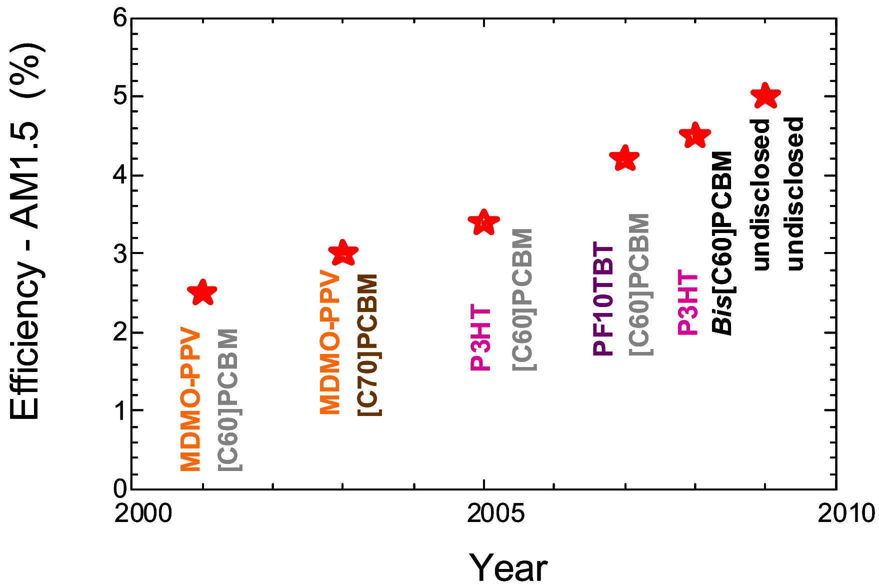
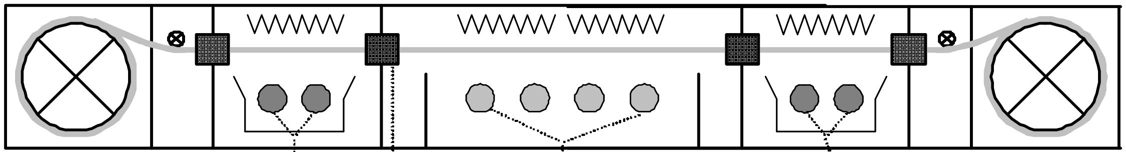
Thin-film photovoltaics

- Organic solar cells



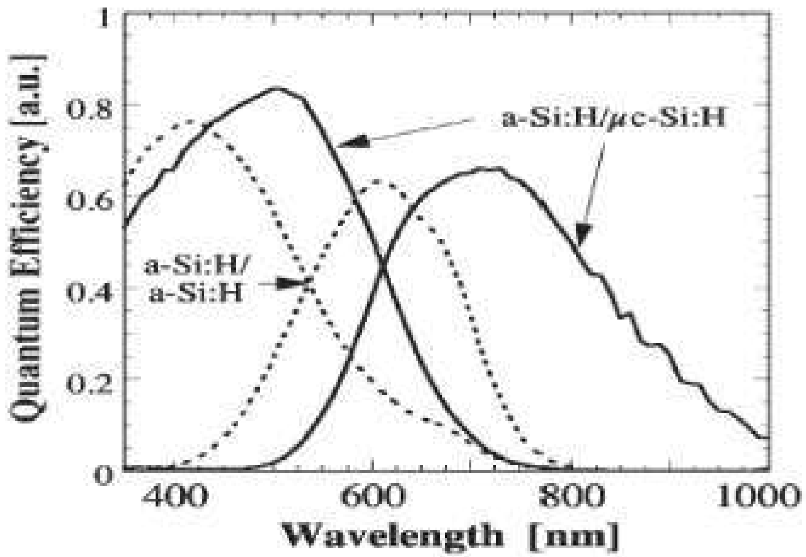


ECN Solar Energy



Thin-film photovoltaics

- Thin-film silicon
  - R-2-R deposition of (n,i,p) silicon on foils
  - Development of thin-film Si tandems



Crystalline Si PV technology

Objective:

- Price of solar electricity in 2015 the same as consumer electricity price, and after that even lower
  - High efficiency
    - 18% module efficiency for crystalline Si PV
  - Reduction of material usage
    - Thin wafers (<150 μm compared to current ~200 μm)
  - Cost effective and environmental friendly processes and products
  - Long lifetime of the modules (>30 yr for crystalline Si)

    - Energy Pay Back Time < 1 yr

Cell structure

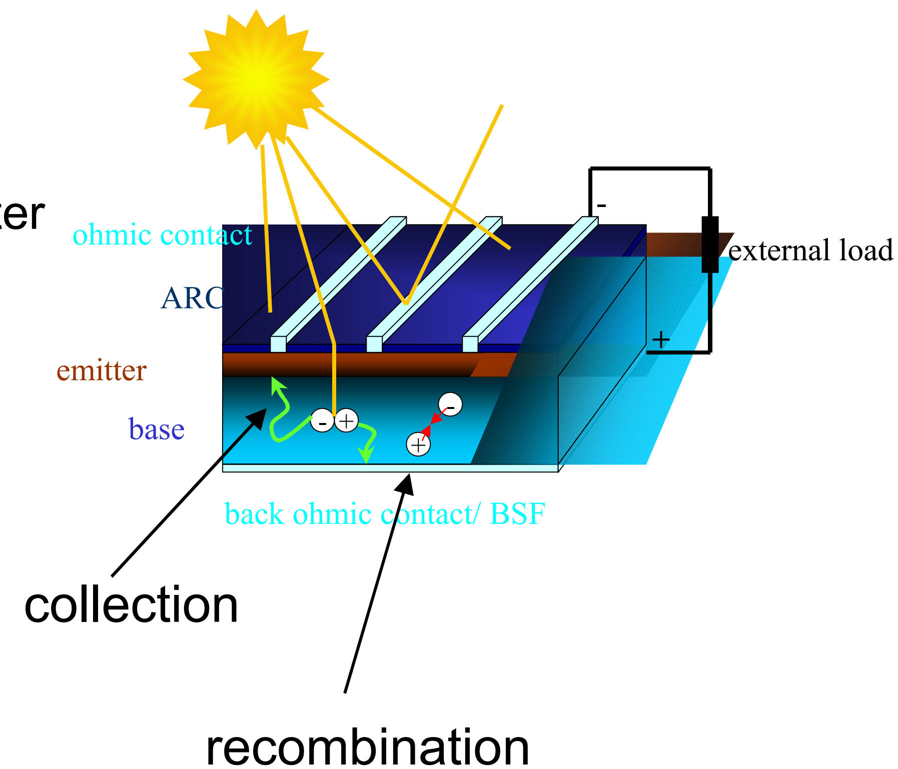
Crystalline silicon solar cell (minority carrier device)

- Base: B doped Si (p-type)
- Emitter: P doped layer (n-type)
  - Recombination losses in base and emitter
  - Voltage over pn junction

- Metallization for contacts
  - Shading losses
  - Resistance losses

- Antireflection coating to enhance current

- Surfaces: recombination losses

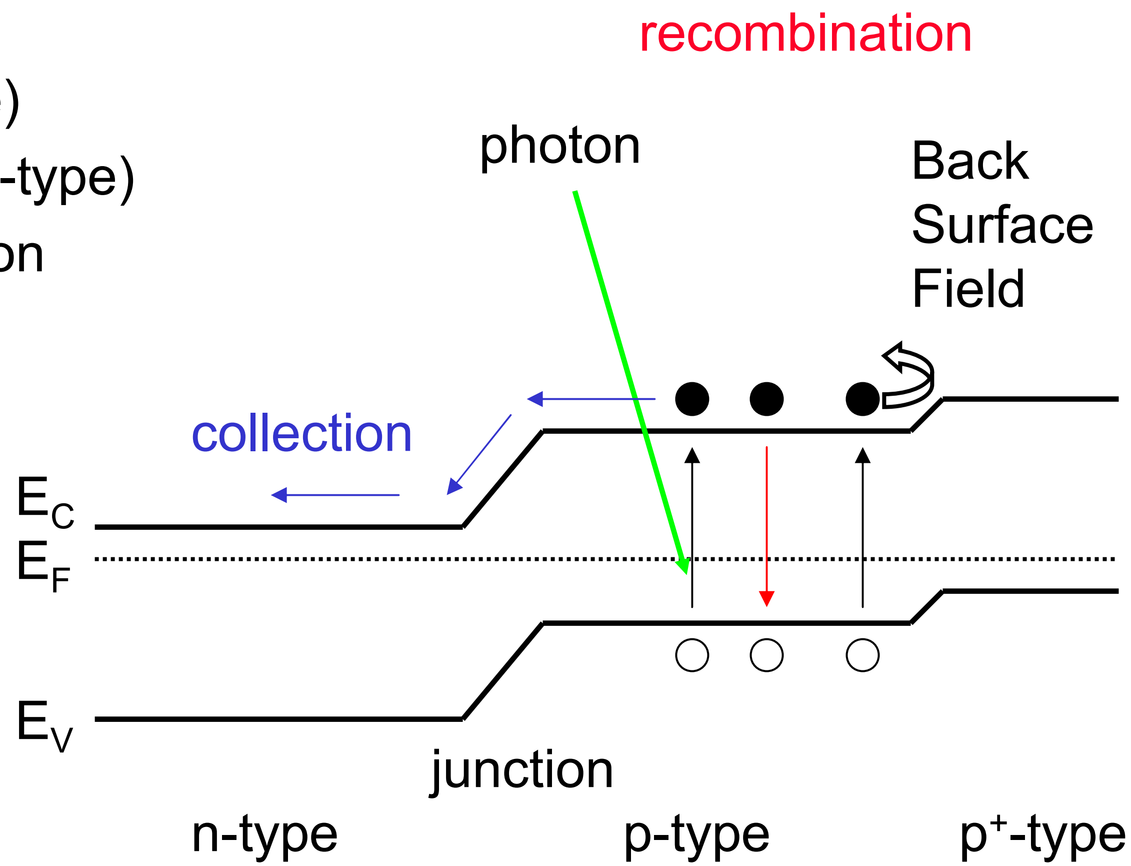


Cell structure

Crystalline silicon solar cell

- Base: B doped Si (p-type)
- Emitter: P doped layer (n-type)
  - Voltage over pn junction
  - Recombination losses

- BSF: p^+ doped layer
  - Highly doped
  - Reduced recombination



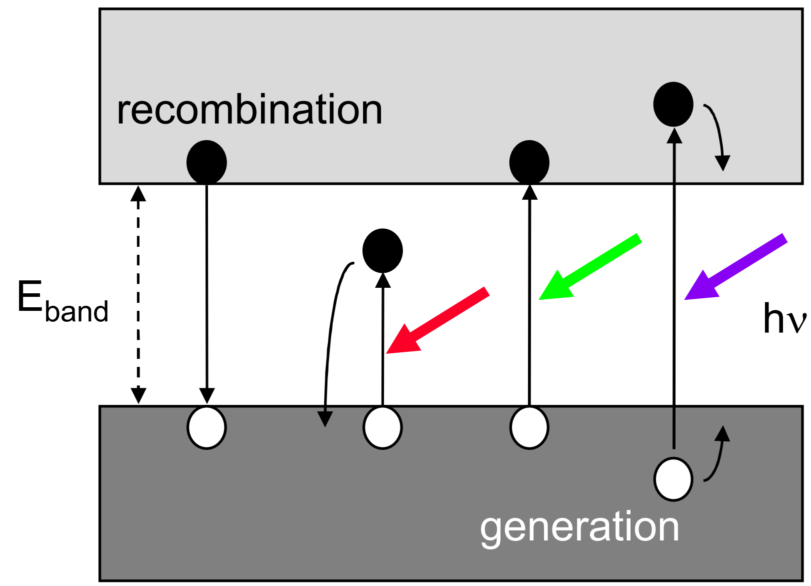
Cell structure

Losses in crystalline silicon solar cell

- Colour mismatch
- Fundamental recombination

} $\eta \leq 30\%$

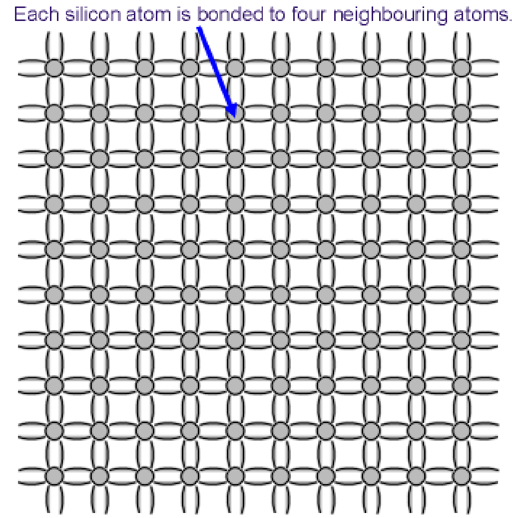
- Additional recombination
  - Impurities, defects, surfaces
- Shading
- Reflection, absorption and transmission
  - Absorption at the rear
- Resistance
- Non-ideal band gap

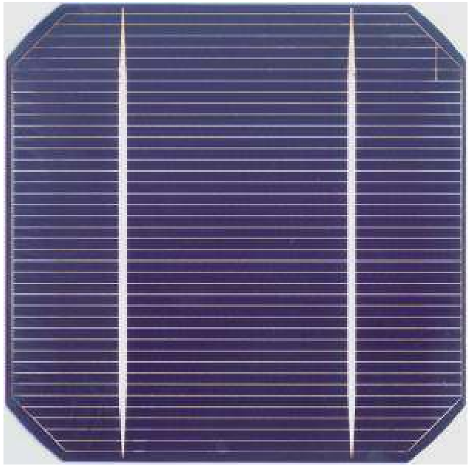


Crystalline Si solar cell: η=13-20%

Crystalline Si PV technology

- Feedstock
  - Effect impurities on cell output
- Wafers
  - Monocrystalline Si
  - Multicrystalline Si
- Cell technology
  - High efficiency with industrial in-line processing
- Module Technology
  - Module design integrated with cell concept
  - Simple interconnection and encapsulation
- Costs and environmental aspects





Crystalline Si PV technology

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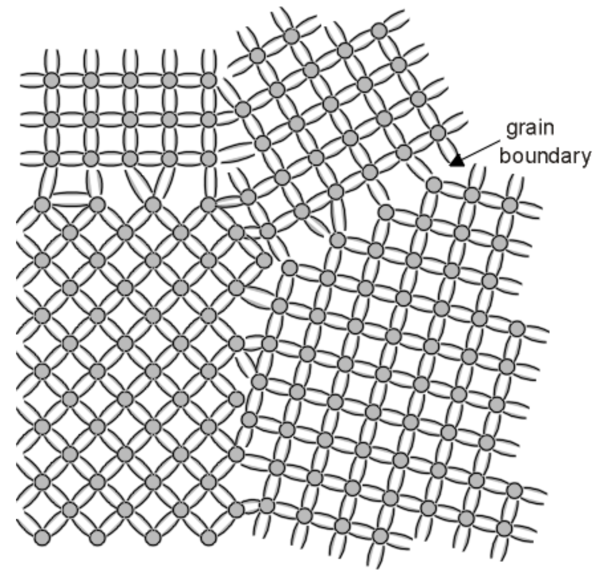
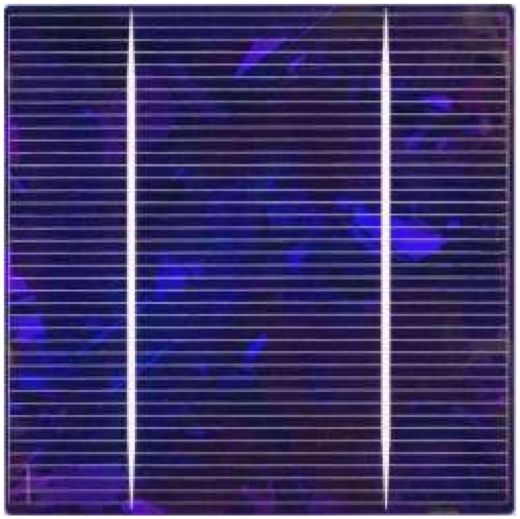
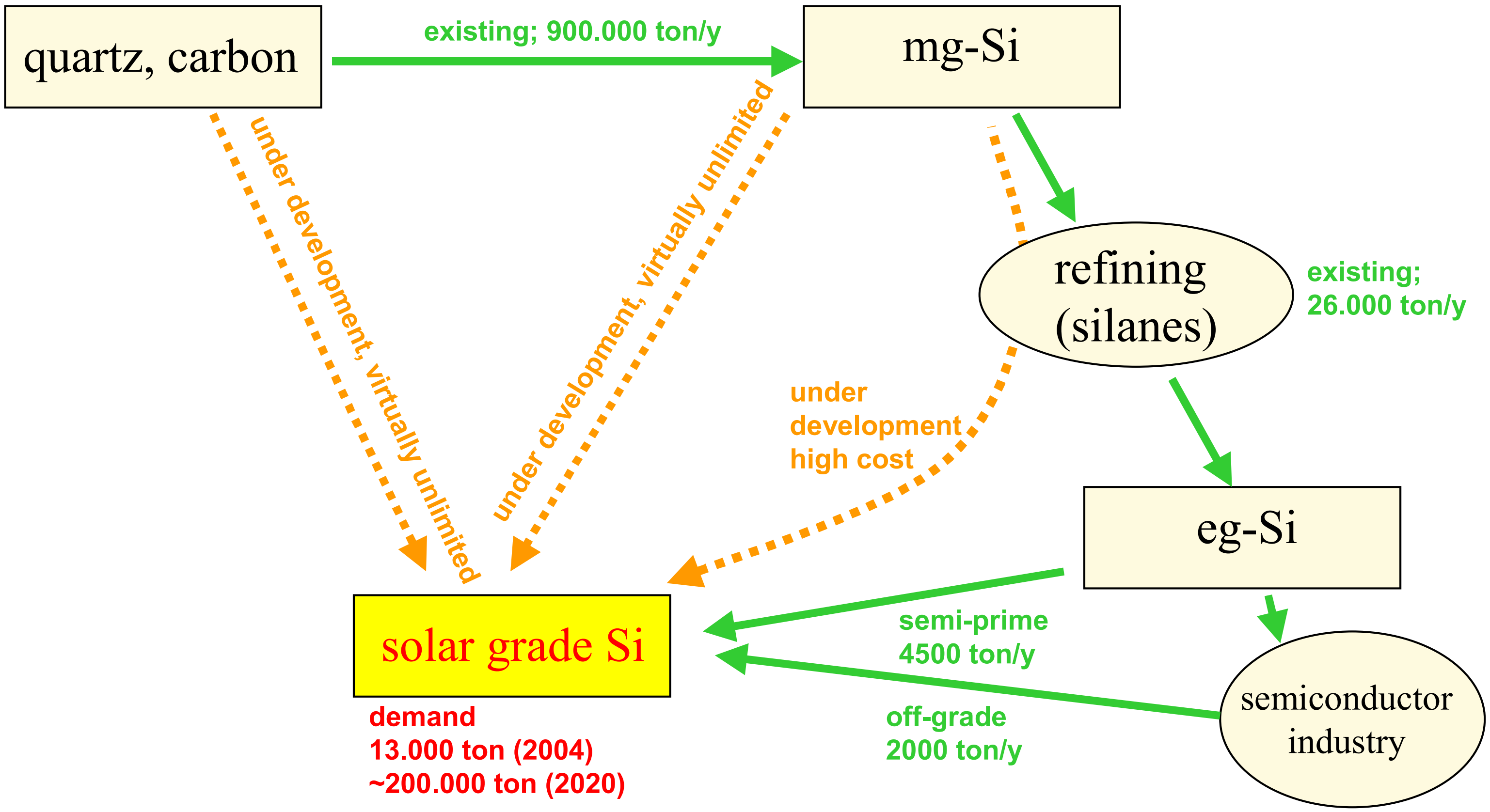




Feedstock production

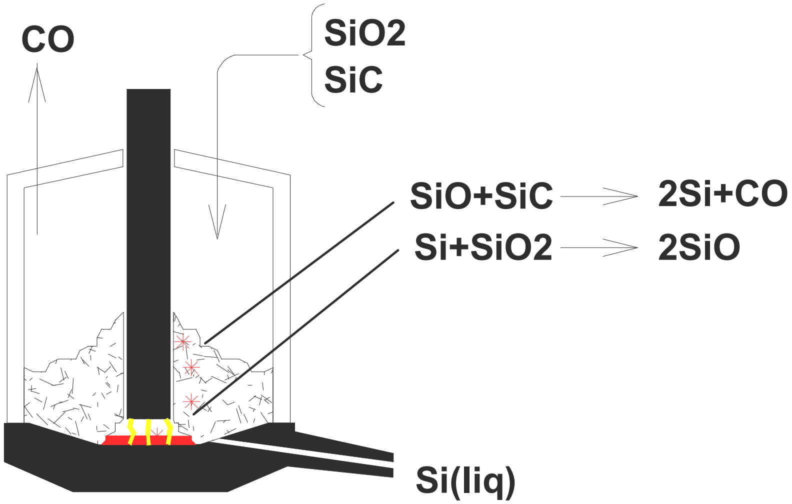


Feedstock production

- Direct route: SOLSILC process

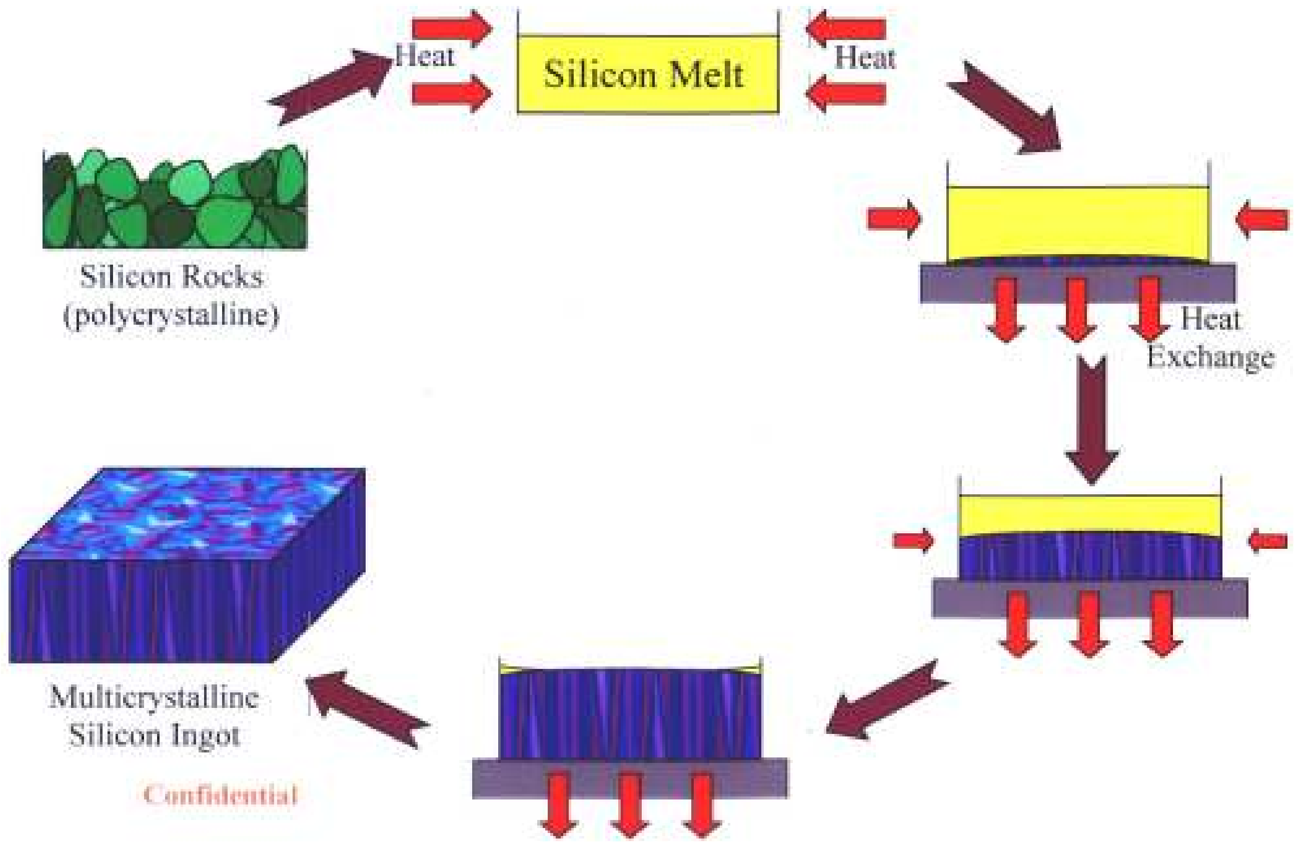
- plasma furnace: SiC from pure SiO_2 and pure C

  pellets of SiC and SiO_2 ⟶ Si(L)



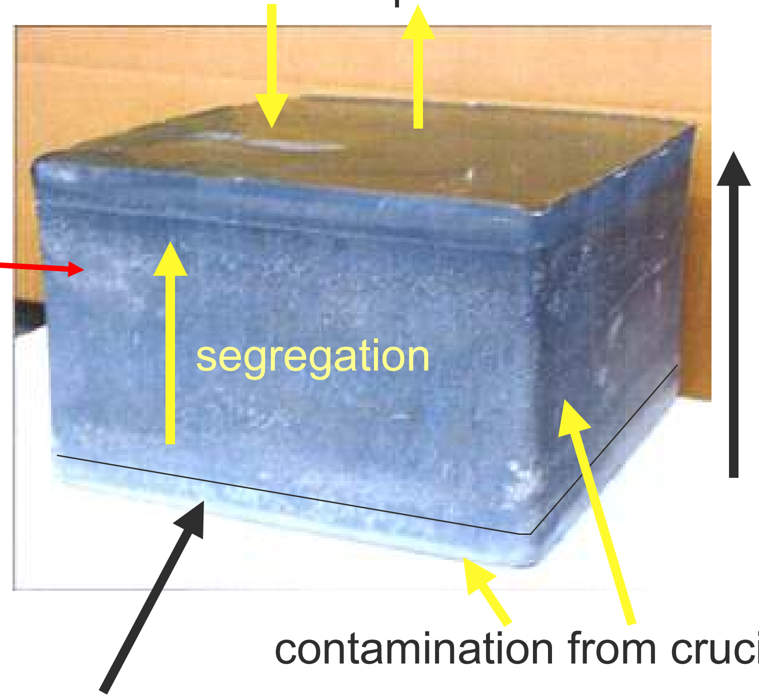
Feedstock: ingot growth

- Multicrystalline Si ingot growth



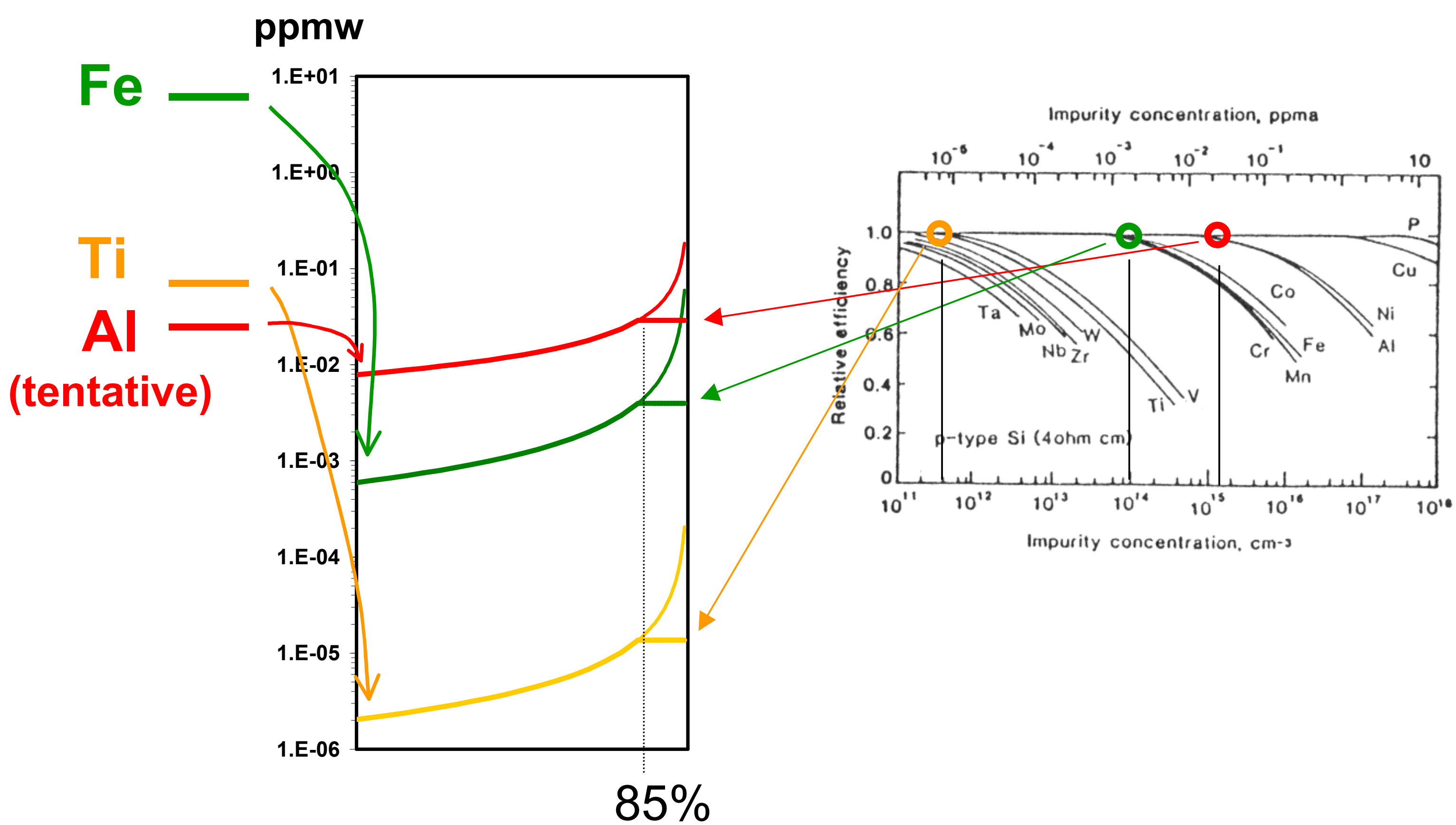
Feedstock: effect impurities

- Feedstock
  - Melting
  - Crystallization
- Ingot
  - Sawing
- Wafer



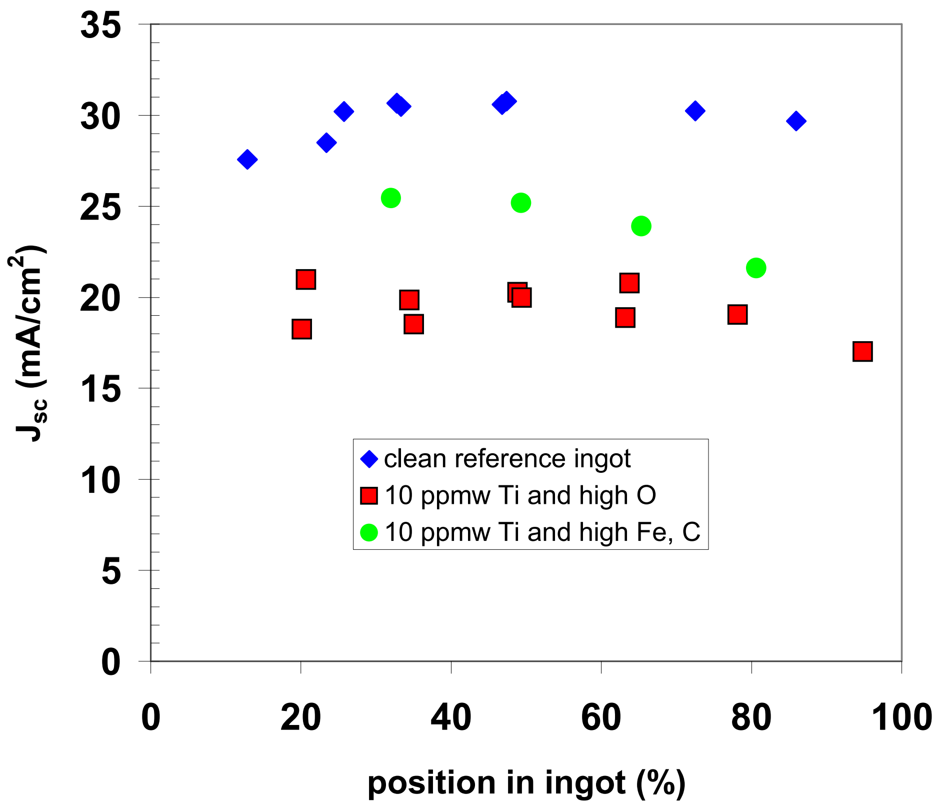
Feedstock: effect impurities

feedstock **ingot** **wafer**



Feedstock: effect impurities

Impurities added to feedstock



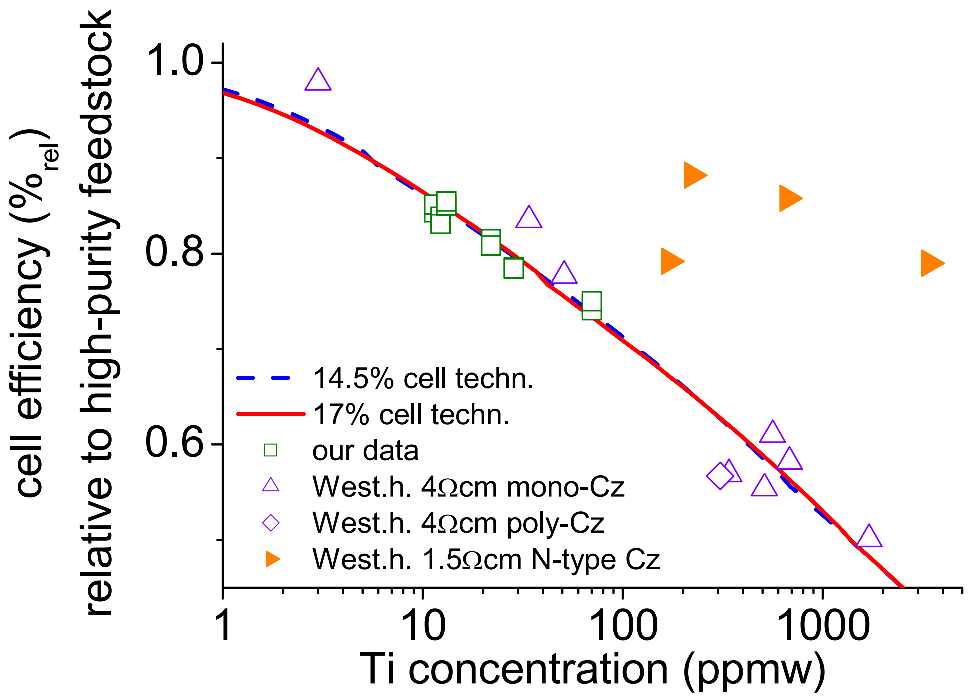
Effect Ti and O on cell output clearly visible

ECN

Feedstock: effect impurities

Impurities added to feedstock

- Ingot growth
- Wafering
- Cell processing
- Characterization
- Model development
  - $1/L_{eff}^2 \propto 1/\tau \propto C_{imp}$
  - Segregation during growth
  - Solar cell modeling



- Needed to define Solar Grade Si

Feedstock: effect impurities

Impurities added to feedstock

- Ingot growth
- Wafering
- Cell processing
- Characterization
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  - $1/L_{eff}^2 \propto 1/\tau \propto C_{imp}$
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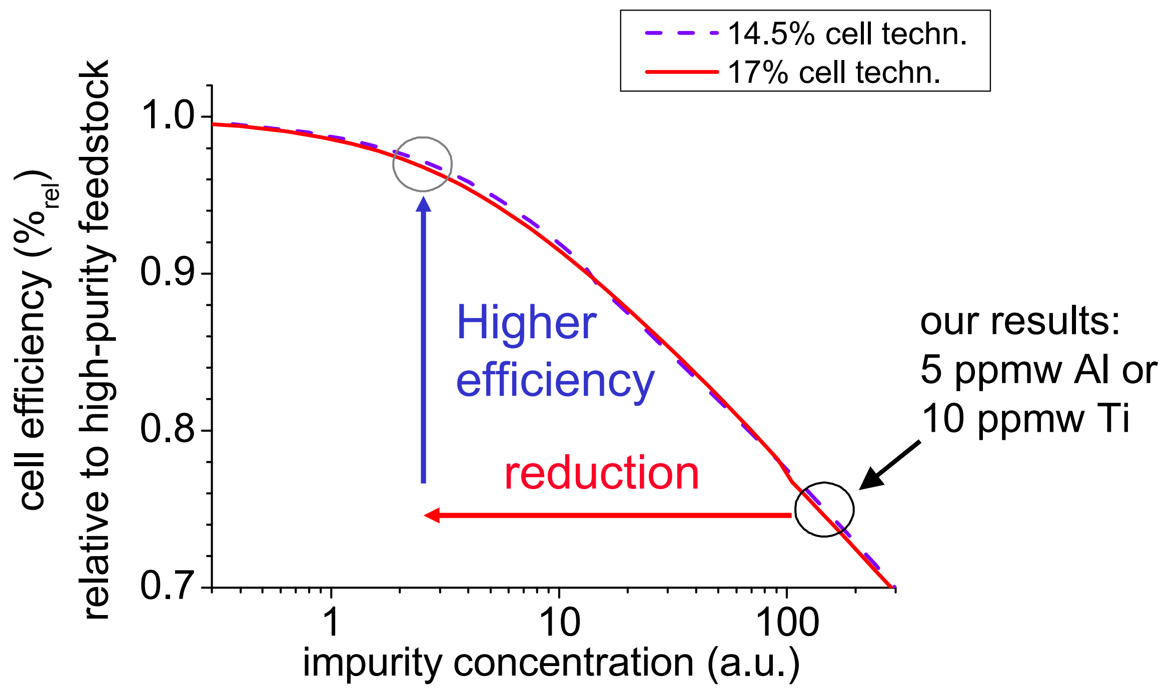
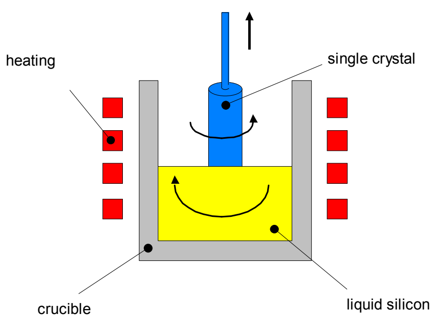


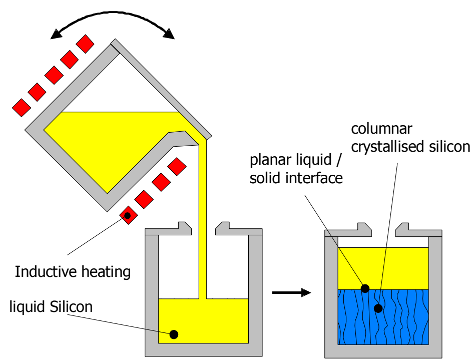
- Needed to define Solar Grade Si

Wafer technologies

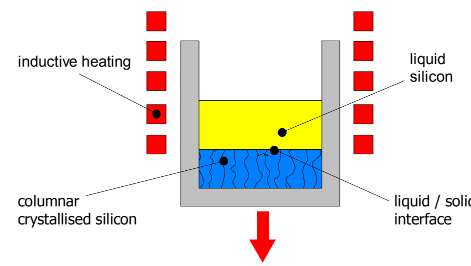
Pulling of Single Crystals (Czochralski)



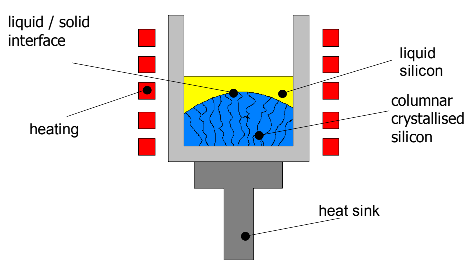
Casting of Silicon Blocks



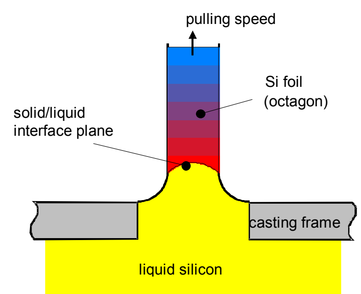
Bridgman Solidification



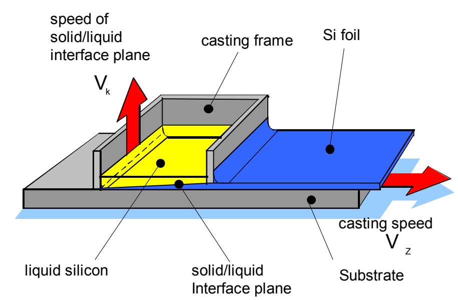
Heat Exchange Method



Edge defined Film fed Growth

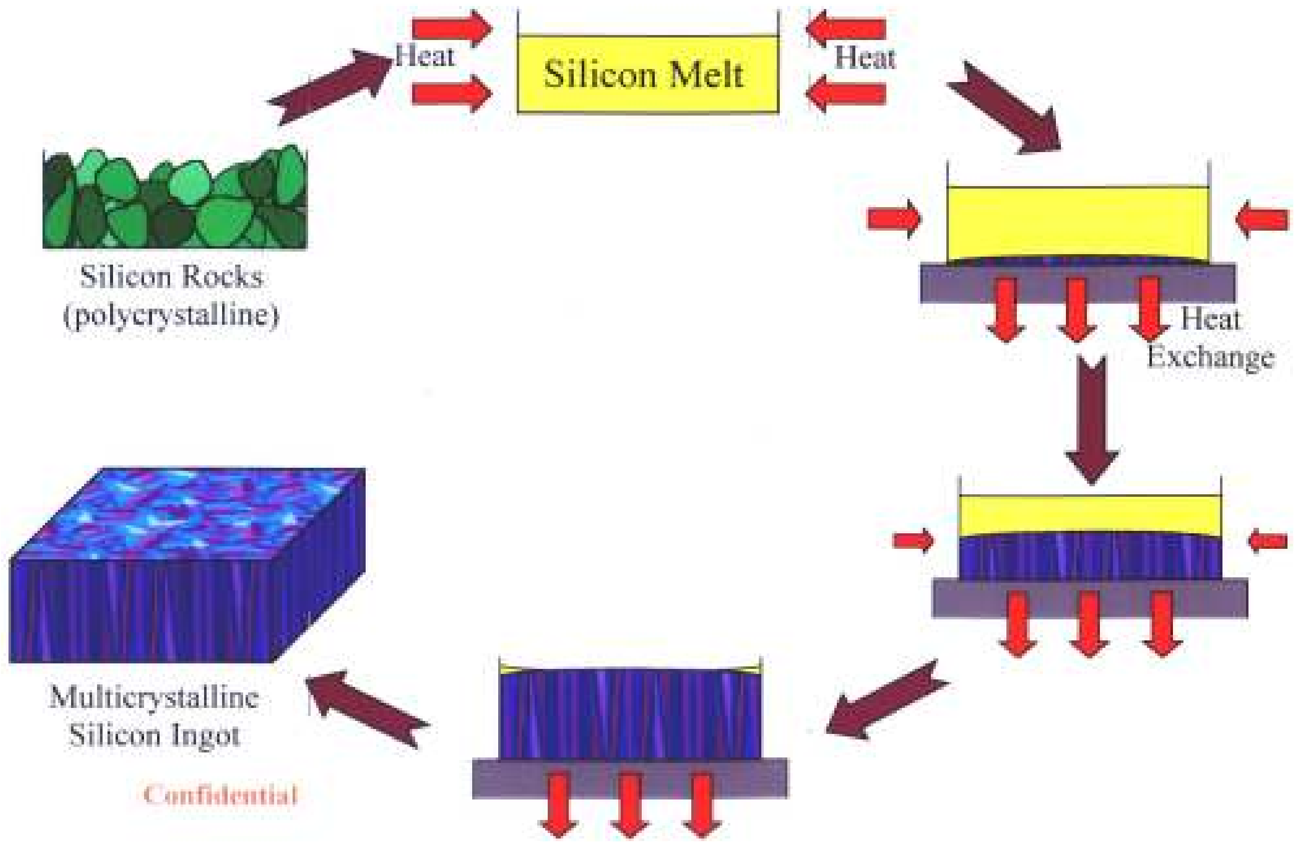


Ribbon Growth on Substrate



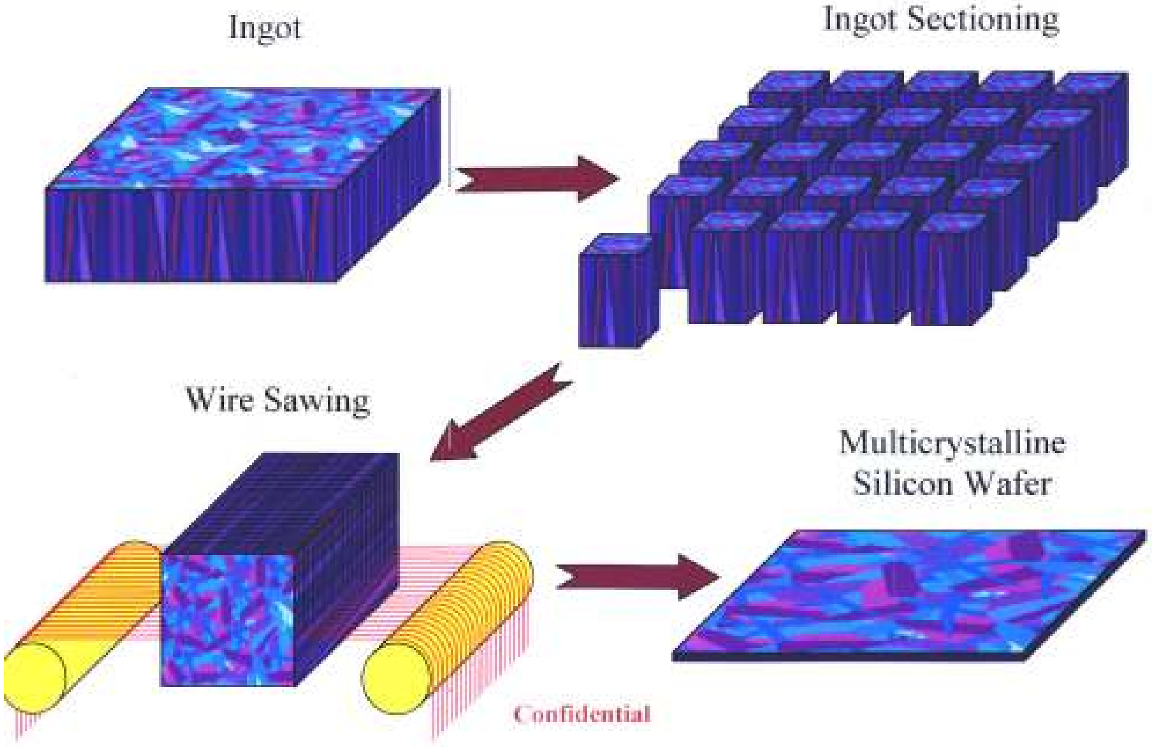
Wafer technologies

- Multicrystalline Si ingot growth



Wafer technologies

- From ingot to mc-Si wafer



Wafer technologies

- High quality monocrystalline Si material
  - Low impurity concentration
  - Low defect concentration
  - Higher efficiency (15-17% in industry, 20% pilot)
  - Higher costs per cell

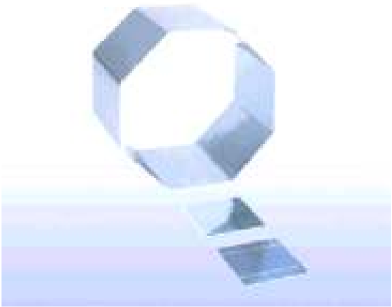
- Lower quality multicrystalline Si material (mc-Si)
  - Higher impurity concentration
  - More defects
  - Lower efficiency (13-15% in industry, >16% pilot)
  - Lower costs per cell

- For both technologies: high sawing losses (about 50%!)

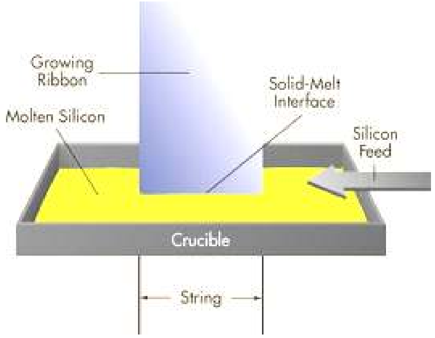
Wafer technologies

- Ribbon technologies (multicrystalline Si)

- Substrate growing and crystallization in the same direction



Edge defined Film-fed Growth (SCHOTT Solar)

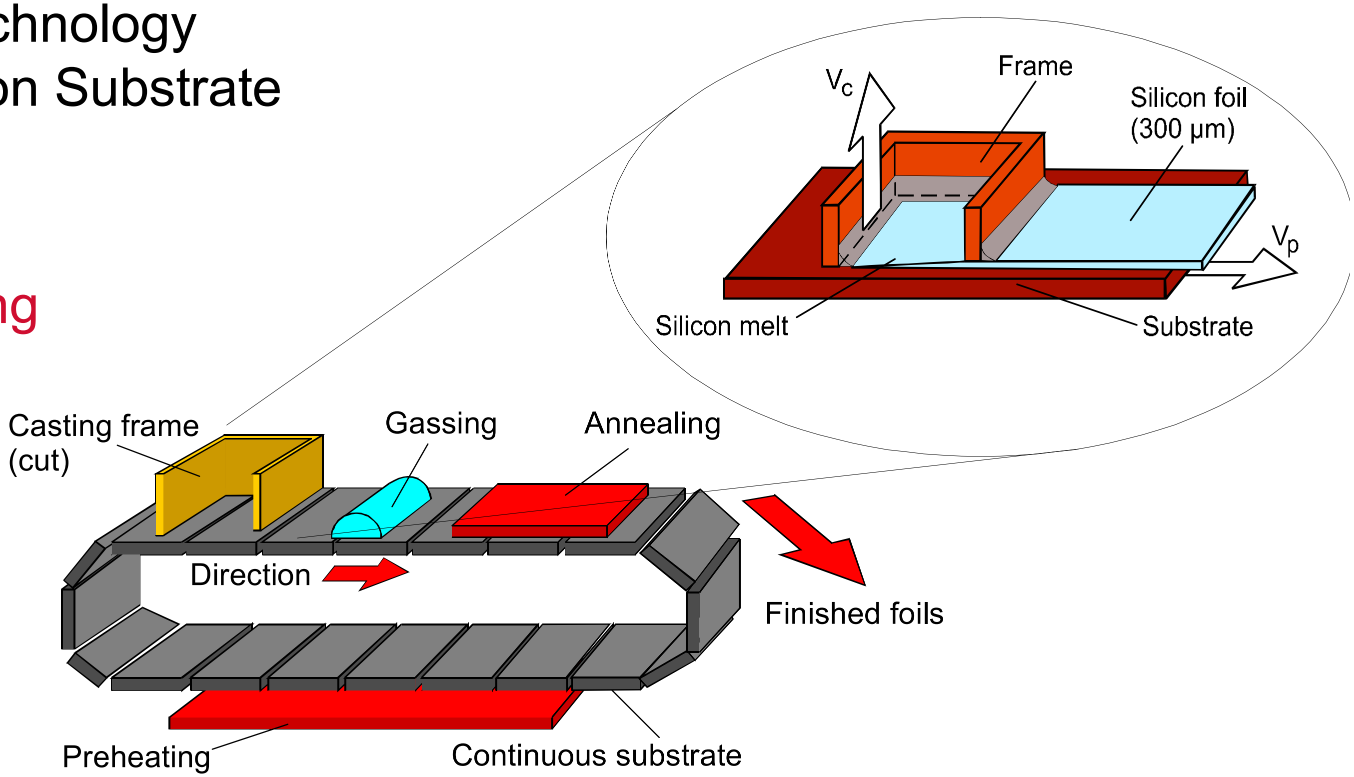


String Ribbon

Wafer technologies

- ECN's ribbon technology
  Ribbon Growth on Substrate
  RGS

- Substrate growing perpendicular to crystallization



Wafer technologies

- ECN's ribbon technology
  Ribbon Growth on Substrate
  RGS

- Substrate growing perpendicular to crystallization

Wafer technologies

Ribbons:

- Better use of Si material (about factor 2)

But

- Lower initial material quality
- Lower efficiencies

- EFG/SR: about 14% (industry)
- RGS: about 13% (lab)
  - Very high throughput

Material	Pull Speed [cm/min]	Through-put [cm^2/min]	Furnaces per 100 MW
EFG	1.7	165	100
SR	1-2	5-16	1175
RGS	600	7500	2-3

*[J. Kalejs, E-MRS 2001 Strasbourg]

Wafer Technology

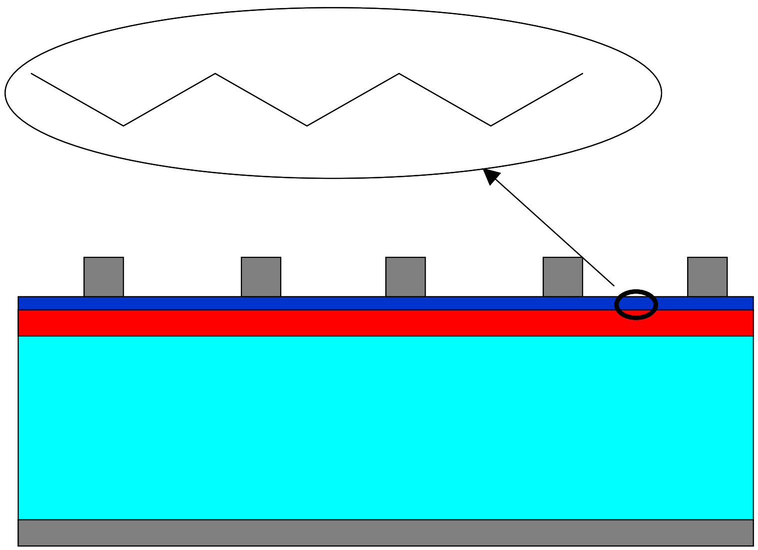
RGS cell efficiencies using industrial process

- Average efficiency 12.5%.
- Current top efficiency 13%[confirmed]
- High efficiency lab processing 14.4%[confirmed]

- ~100 µm thin RGS wafer made
  - Efficiency around 11%
  - 2.9 g Si/Wp (nowadays ~10 g Si/Wp)

Cell processing

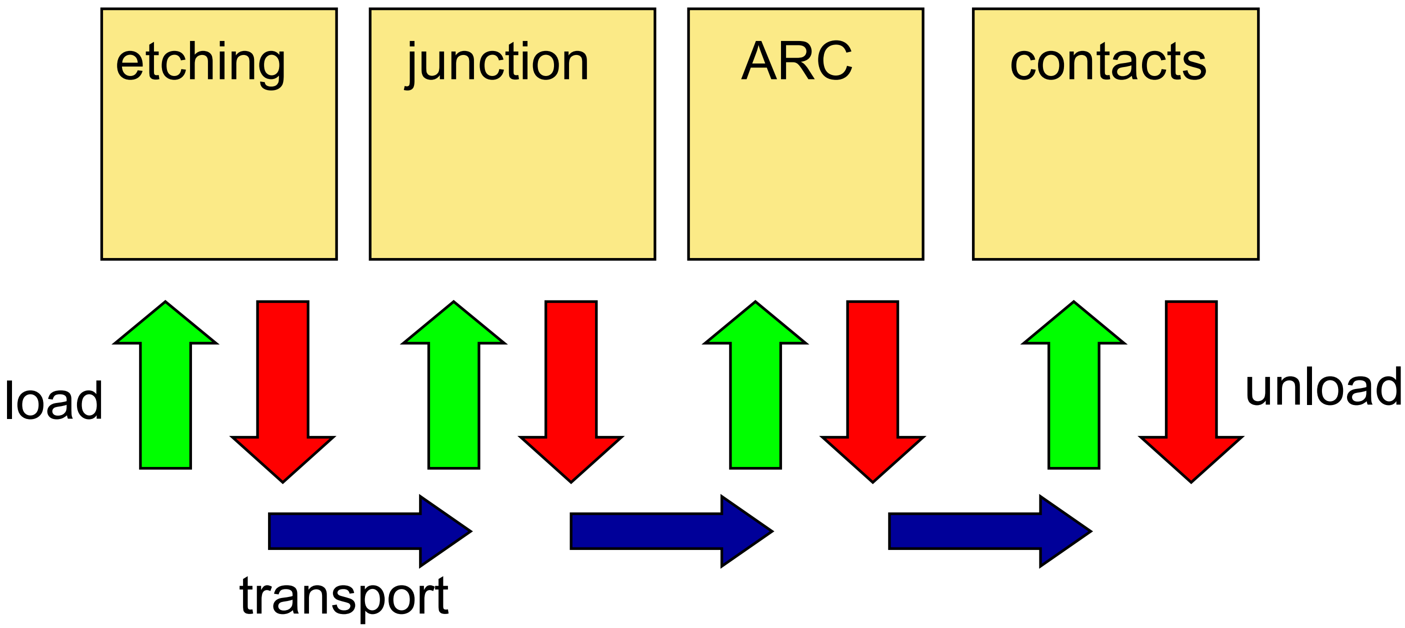
- Saw damage removal
  - Texturing for enhanced light coupling (better efficiencies)
- Emitter diffusion
  - Material improvement by gettering
- SiN_x deposition as antireflection layer
  - Material improvement by passivation
  - Reduced surface recombination (surface passivation)
- Metallization
  - Ag front side
  - Al rear side (so-called Back Surface Field)
- Sintering for contact formation

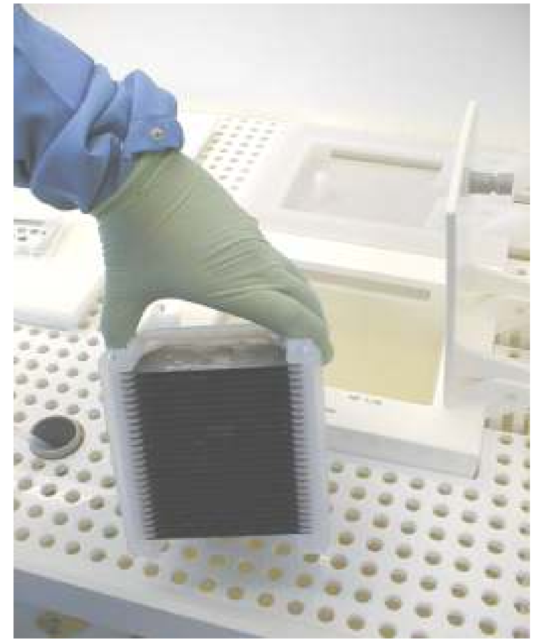


Cell processing

Batch processing

- Wafers in carriers
- Each process step well controlled
- Used for high efficiency processing



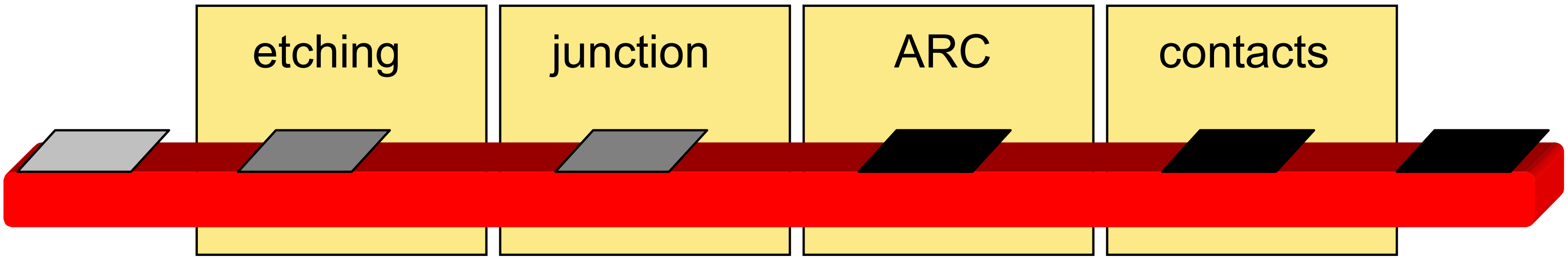


Cell processing

<u>ECN's inline processing</u>

Horizontal wafer transport on belts (wafer in; cell out)

- No wafer carriers
- Large and thin wafers easier to handle (cost reduction)



Cell processing

Examples from industry

Batch processing BP Solar

In-line processing Solland Solar

Cell processing

ECN Baseline process

- Multicrystalline p-type Si
- Acidic texturing / saw damage removal
- P diffusion using belt furnace
- Deposition of SiN_x
- Metallization (Ag front, full Al rear)
- Simultaneous sintering both contacts

Results

Processing complete columns of wafers during two years

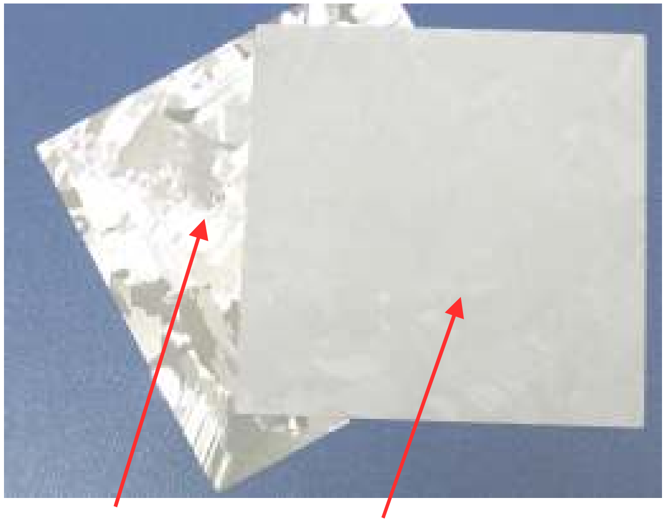
- Average 16%
- In industry 15-16%

Wet chemical etching

Sintering contacts

Texturing

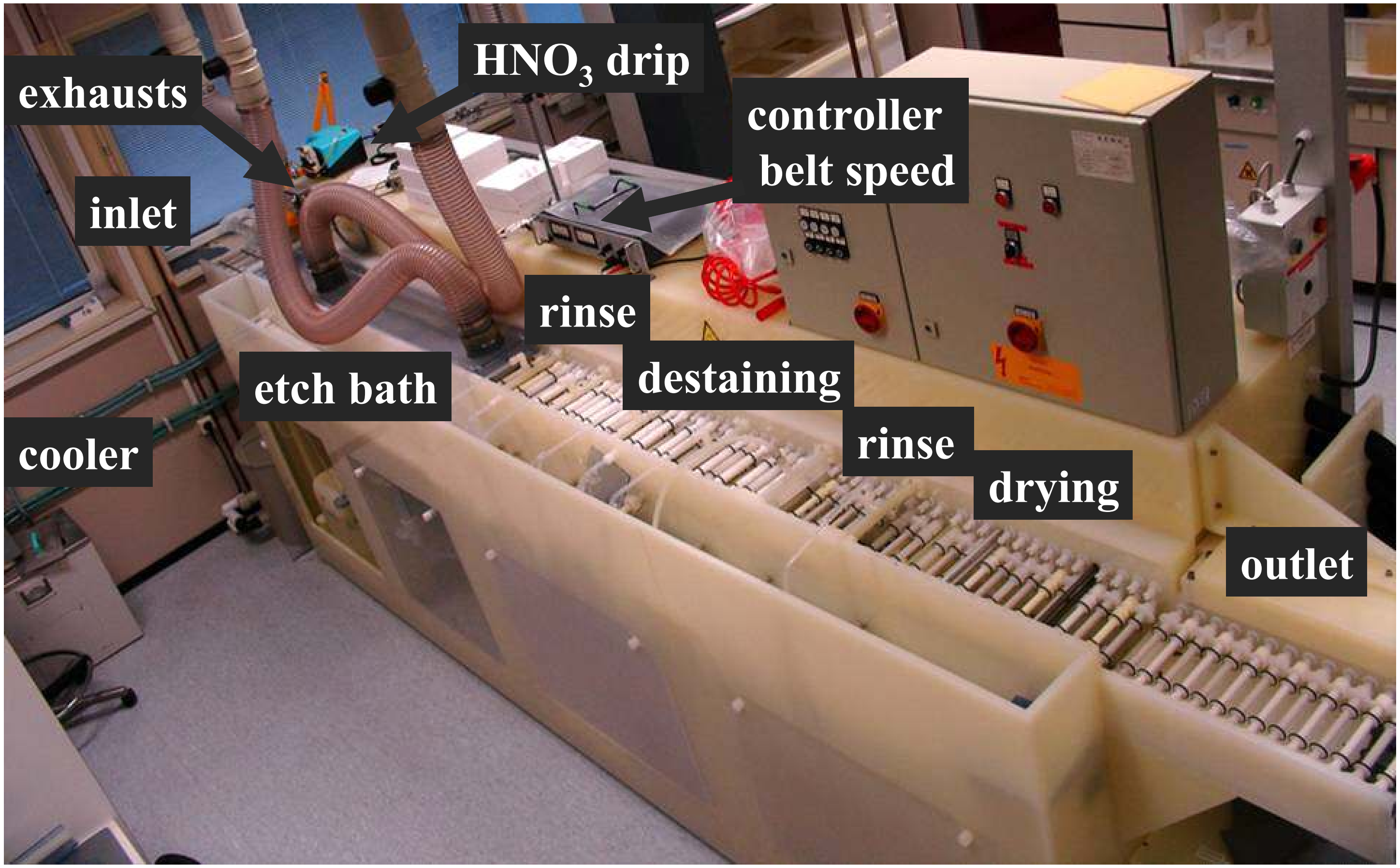
Acidic texturing of mc-Si



Alkaline and acidic etch

Texturing

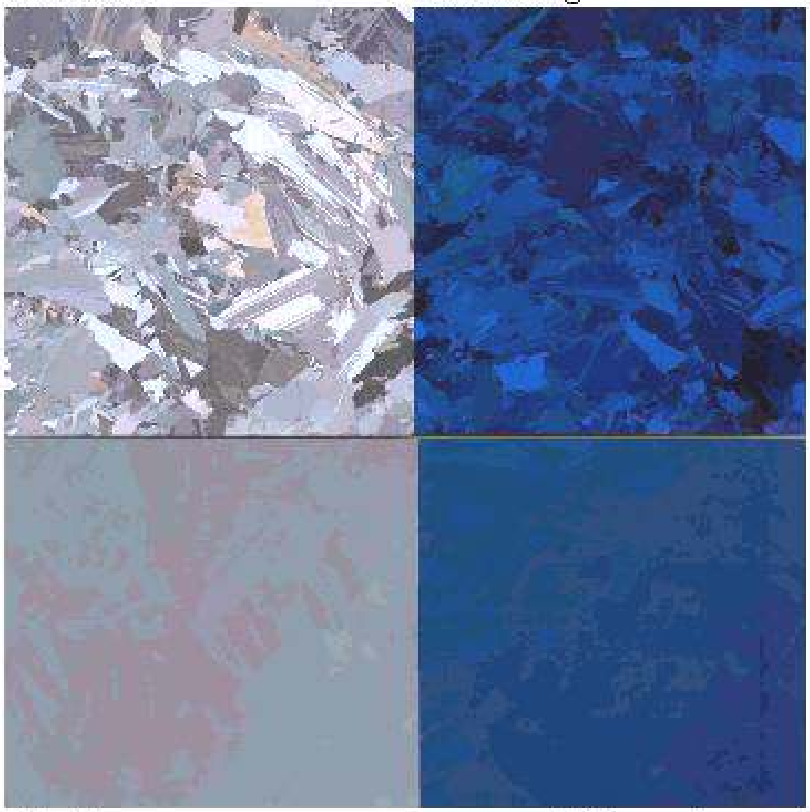
Acidic texturing of mc-Si



Texturing

Acidic texturing of mc-Si

- Lower reflection, higher efficiency
  - About 0.5% absolute
- Better appearance

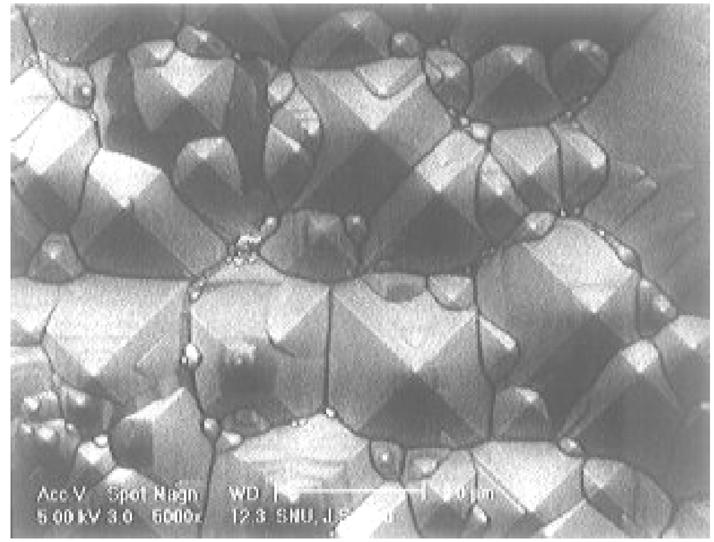


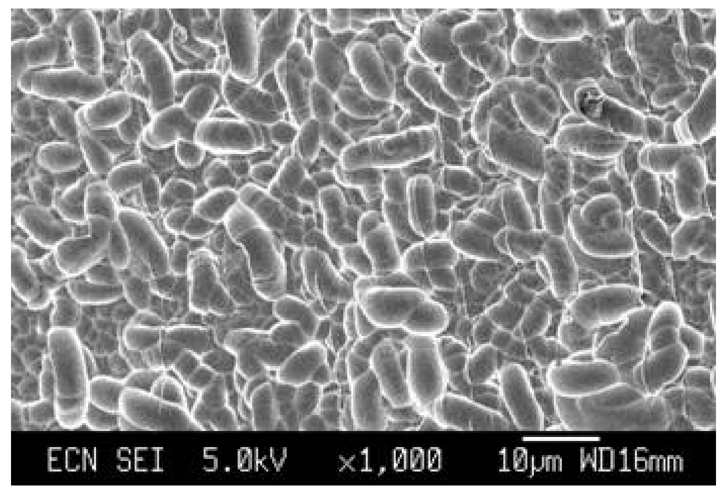
Texturing

Surface structure texturing Si

- Monocrystalline Si
  - Alkaline etching (NaOH or KOH)
  - Anisotropic etching
    - (111) planes slowest etching rate
    - Pyramids on (100) substrates

- Multicrystalline Si
  - HF/HNO_3 etching
  - Isotropic etching
    - Random structure



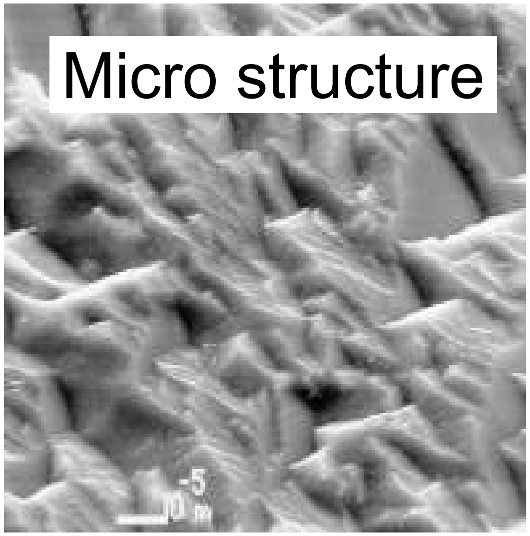


Texturing

Alkaline etching of Si

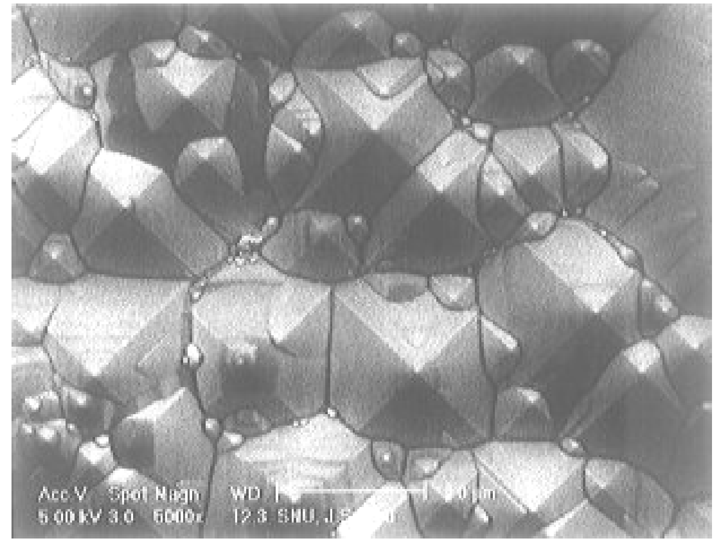
$$Si + OH^- + H_2O \rightarrow SiO_3^{2-} + H_{2\ gas}$$

- Higher concentrations and higher *T*
  - Almost isotropic etching
  - High etching rate
  - Used to remove saw damage (5-10 μm)
  - High reflectance (~30%)

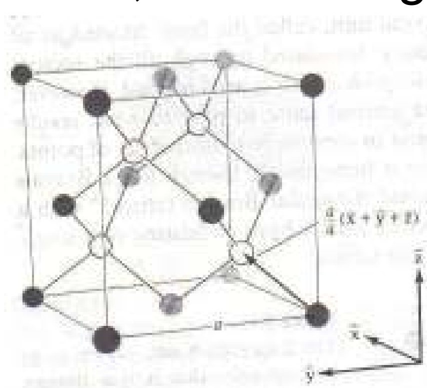


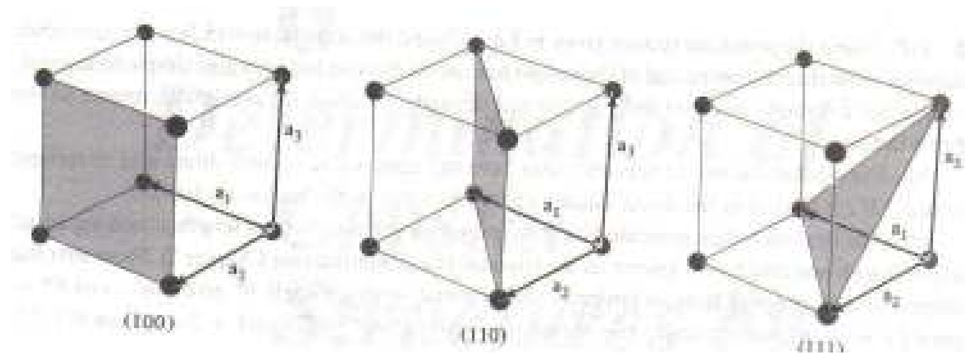
Texturing

Alkaline etching of Si



- Lower concentrations and lower *T*
  - Anisotropic etching
    - (111) planes slowest etching rate
    - Pyramids as texture on (100) substrates
    - Low reflectance (~10%)
  - But, low etching rate





Texturing

Acidic etching of Si

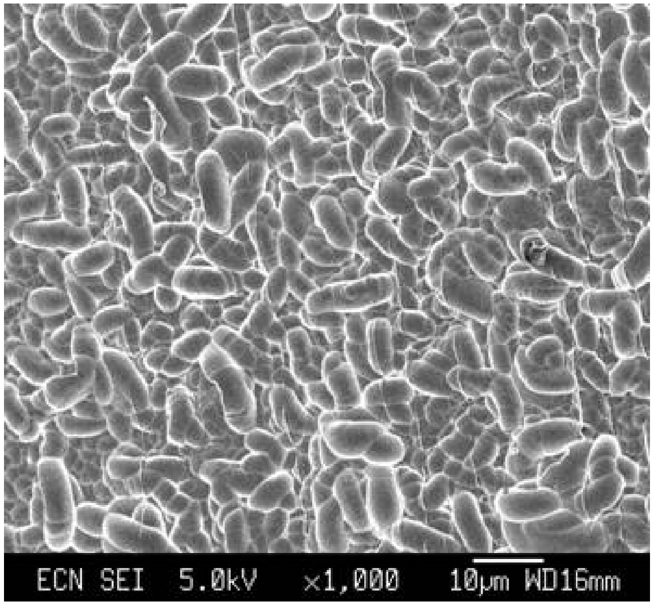
Mixture HF/HNO_3

Oxidation

$$3\ Si + 4\ HNO_3 \rightarrow 3\ SiO_2 + 4\ NO_{gas} + 2\ H_2O$$

Oxide removal

$$SiO_2 + 4\ HF \rightarrow SiF_{4\ gas} + 2\ H_2O$$



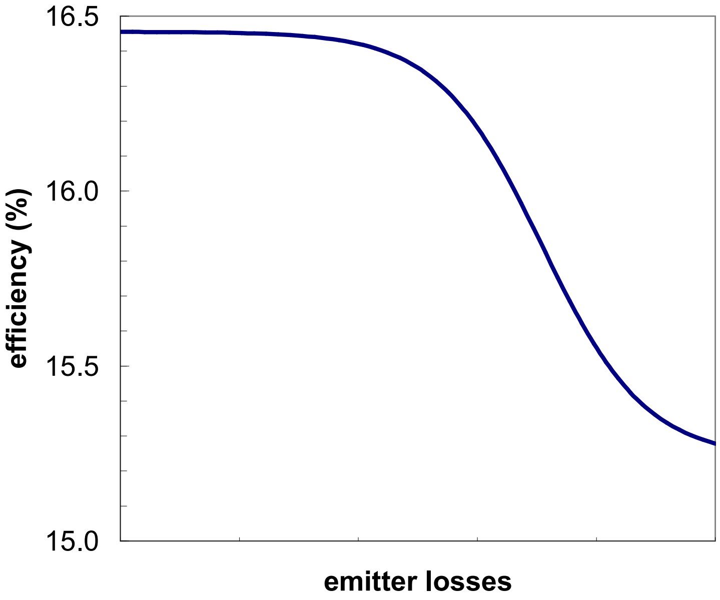
- Obtained surface morphology depends on composition
  - Polishing
  - Defect etching
  - Texturing

Emitter processing

Needed to form p-n junction

- Apply P source
- Diffusion at ~900 C for about 10 minutes

- Depth about 0.5 μm
- P concentration at surface: > 2×10^{20} cm^{-3}
  - Higher concentration needed for good contacting
  - However, it will result in additional recombination losses

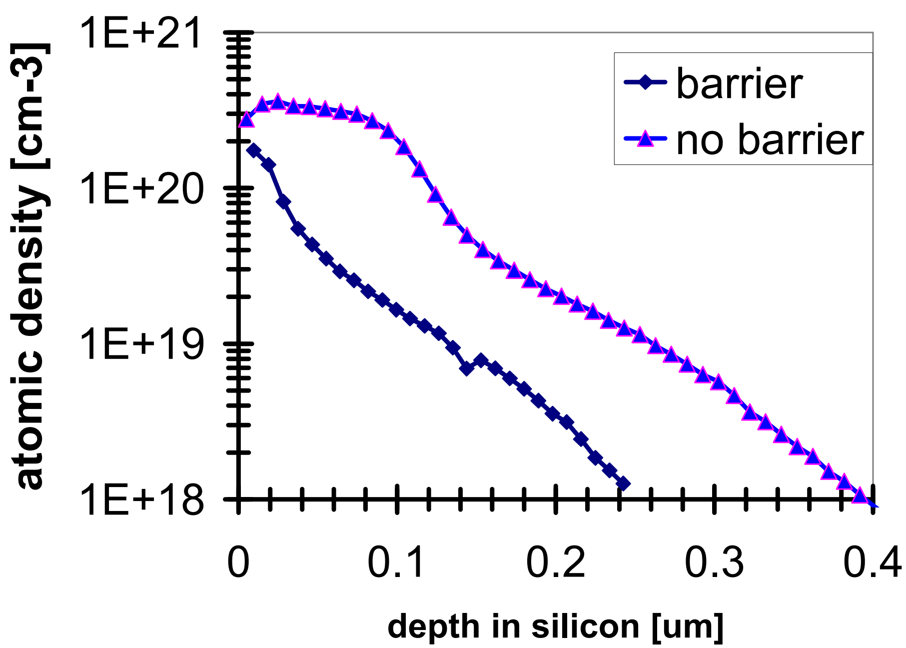


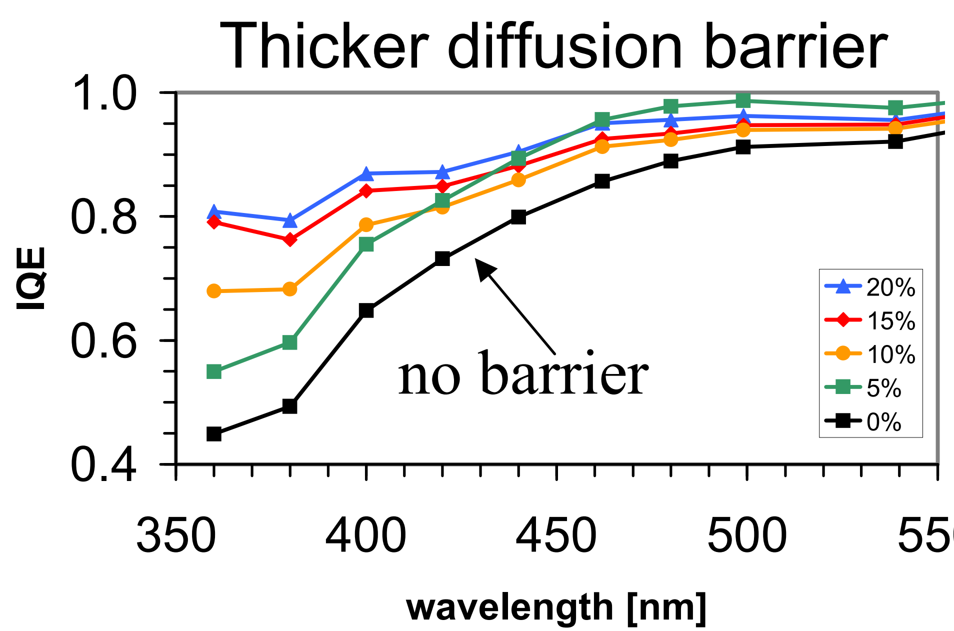
Improved emitter/front side processing can give an efficiency gain of more than 0.5% absolute

Emitter processing

Effect dopant concentration on IQE

- Improved blue response (up to 550 nm) for lower dopant concentration
- Higher V_{oc} and higher J_{sc}: higher efficiency!



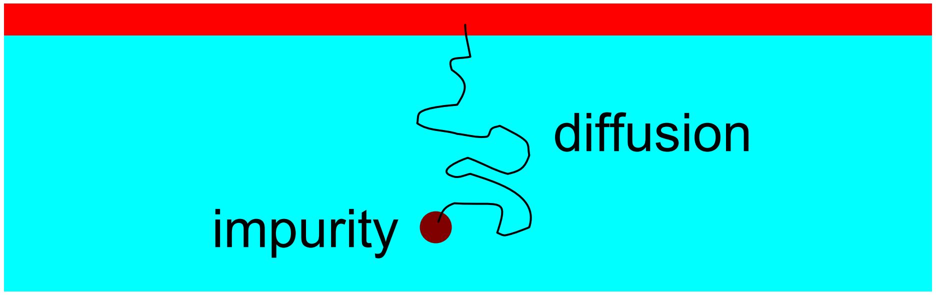


Emitter processing

Additional effect of emitter processing

- So-called gettering
  - Diffusion of impurities to P rich layers (P-gettering)
  - Impurities will not affect efficiency in those P rich layers

- Improved bulk quality and, thus, higher efficiency



SiN_x deposition

Applied using chemical vapour deposition

- Low pressure chemical vapour deposition (only surface passivation, ~700 C)
- Plasma enhanced chemical vapour deposition (different systems, ~400 C, 0.5-10 nm/s)
- Sputtering (several nm/s)

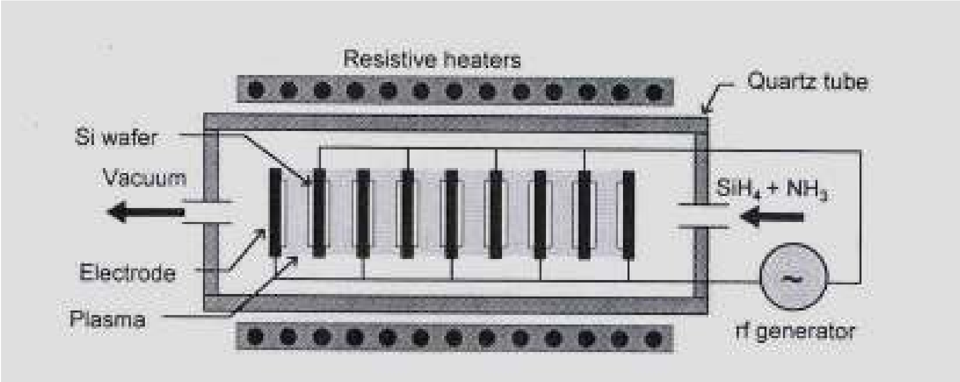
Functions SiN_x:H layer

- Antireflection coating (70-80 nm)
- Surface passivation (reduced recombination at the surface)
- Bulk passivation (improved material quality)
  - During anneal H diffuses into bulk and makes defects/impurities electrically inactive

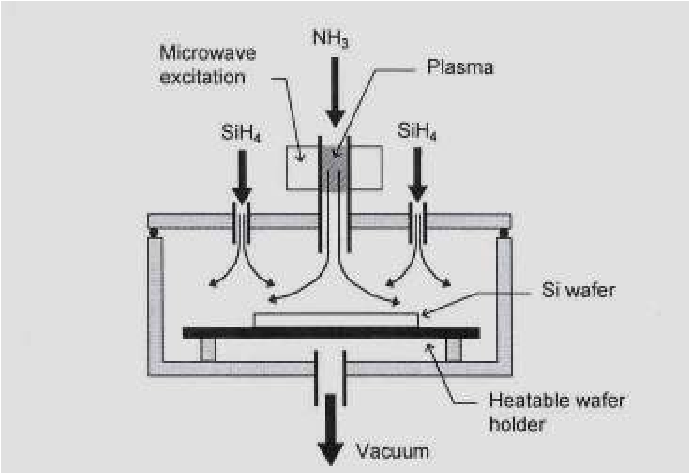
SiN_x deposition

Plasma Enhanced Chemical Vapour Deposition (PECVD)

- Parallel plate system
  Direct plasma
  - Wafers as electrodes
  - Ion bombardment dependent on plasma frequency
  - Damaged layer



- Remote PECVD
  - No ion bombardment

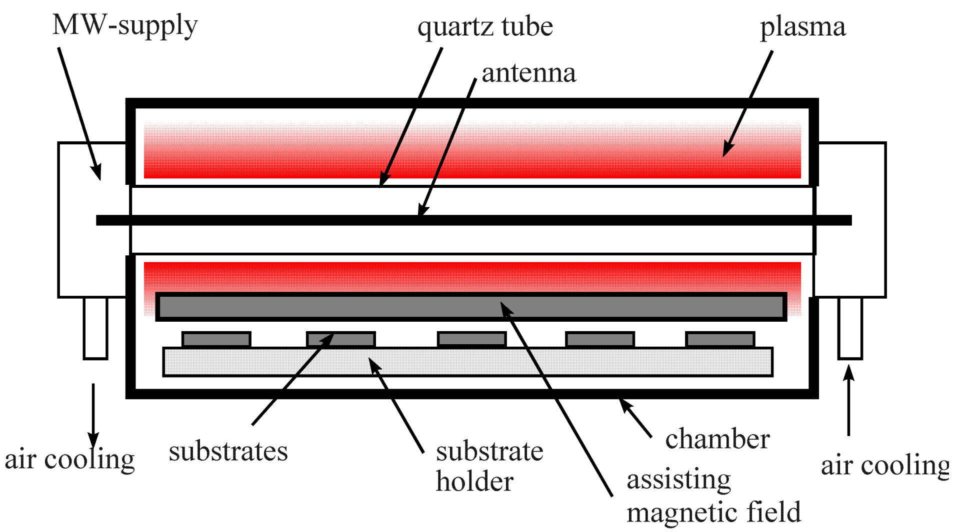


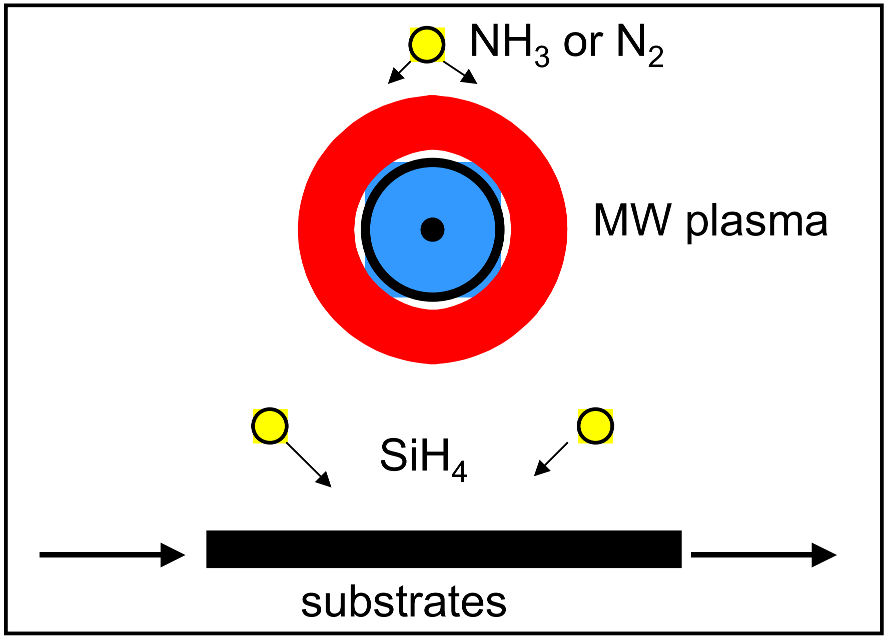
Aberle et al.

SiN_x deposition

ECN's MicroWave Remote PECVD

- Deposition rate about 1 nm/s

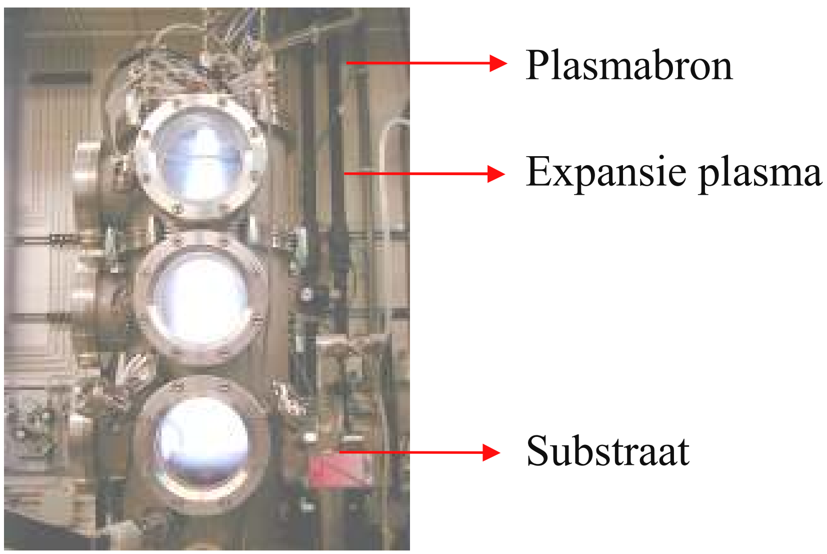


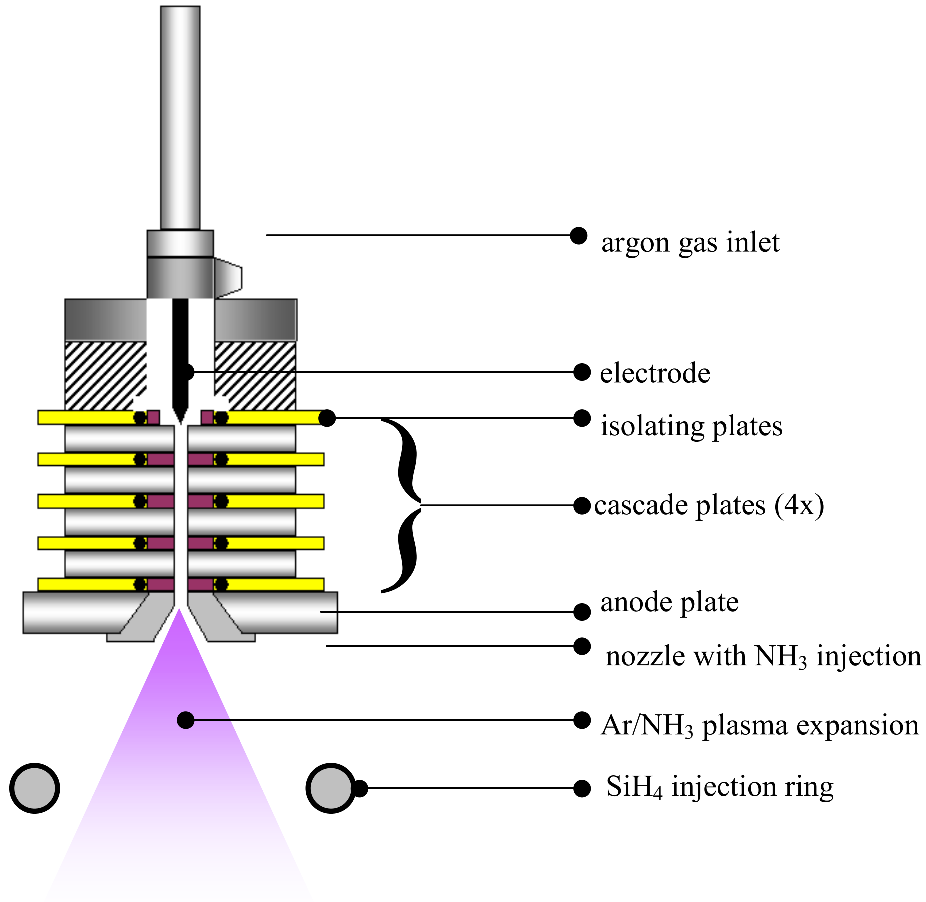


SiN_x deposition

Expanding Thermal Plasma (ETP)

- Developed by TU/e
- Deposition rate 5-10 nm/s
- TU Delft: for thin film Si depositions

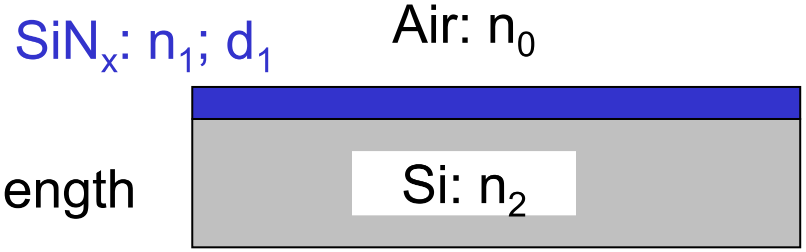




SiN_x deposition

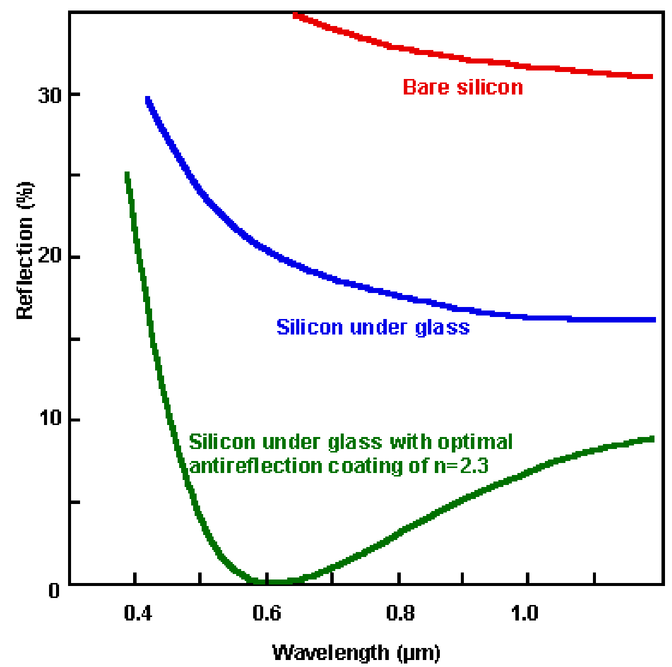
Optical specifications SiN_x:H layer

- Refractive index: *n*=2.1
  higher *n* causes absorption at lower wavelength



$$n_1 = \sqrt{n_0 n_2} \qquad d_1 = \frac{\lambda_0}{4 n_1}$$

- Ideal for air-Si: *n*=1.9; d=~80 nm
- Ideal for air-glass-Si: *n*=2.3; d=~65 nm
  (absorption SiN_x too high)

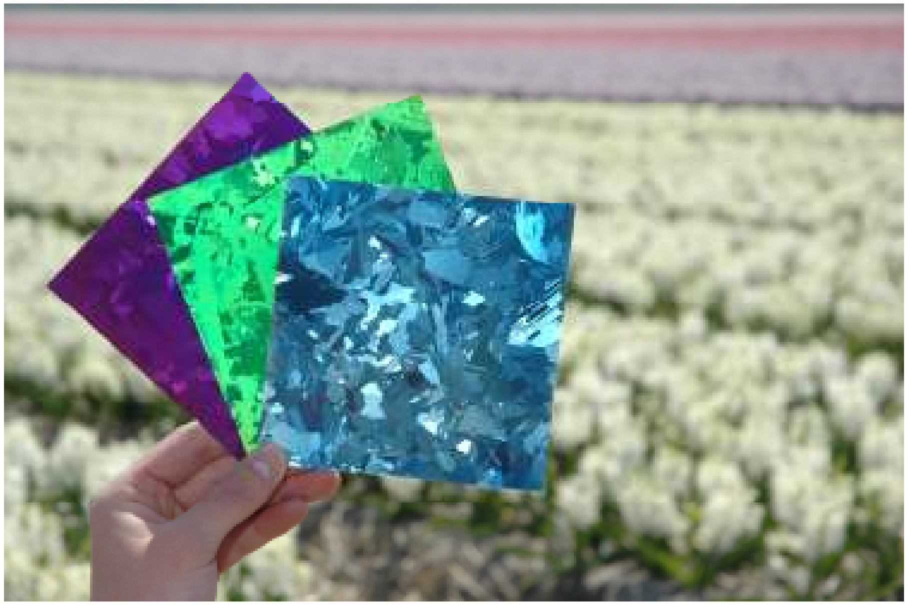


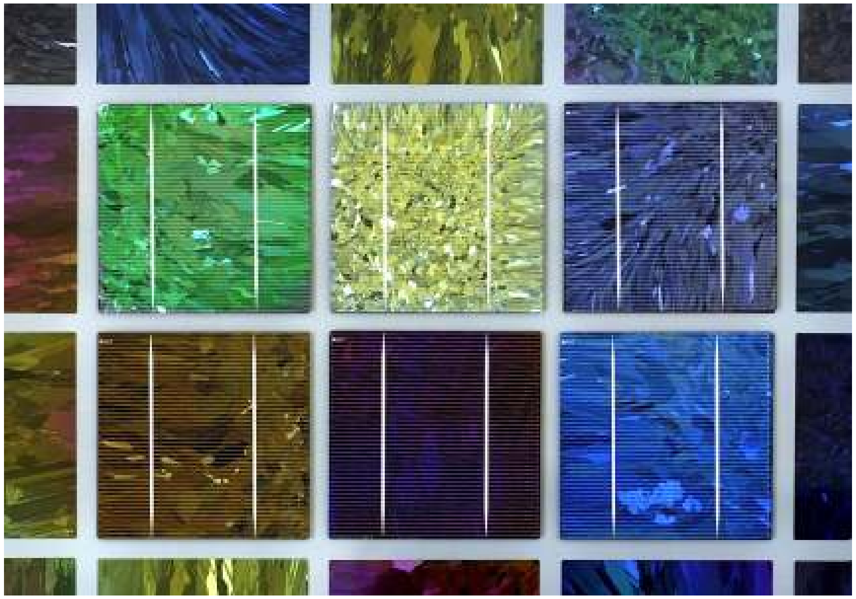
- *n* can be tuned with gas composition
- Higher *n*: more Si (SiH_4)
- Lower *n*: more N (NH_3)

SiN_x deposition

Optical specifications SiN_x:H layer

- Different layer thickness: different colour



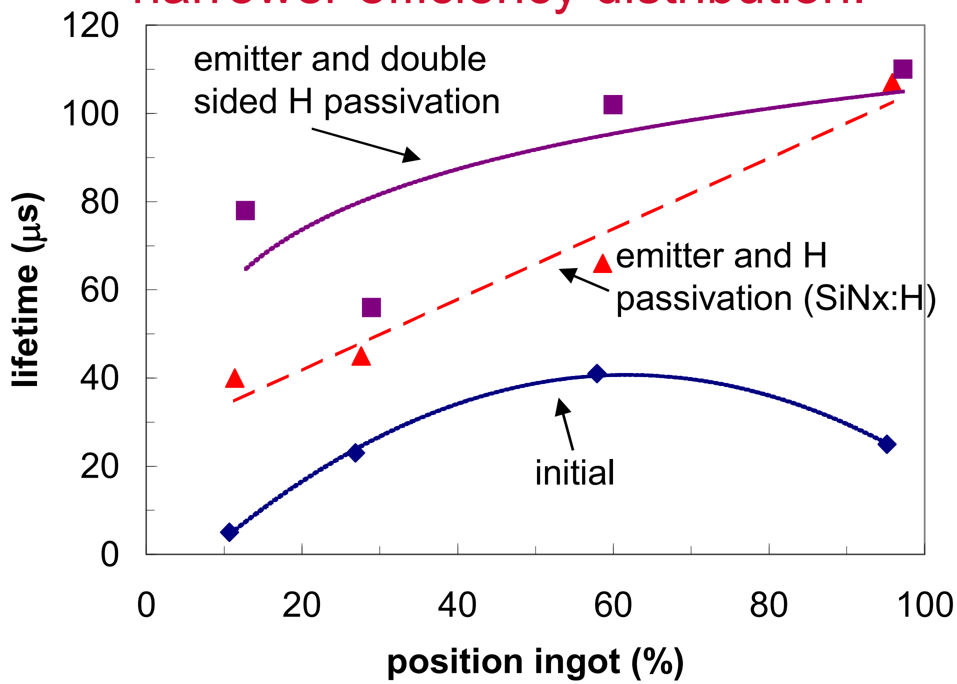


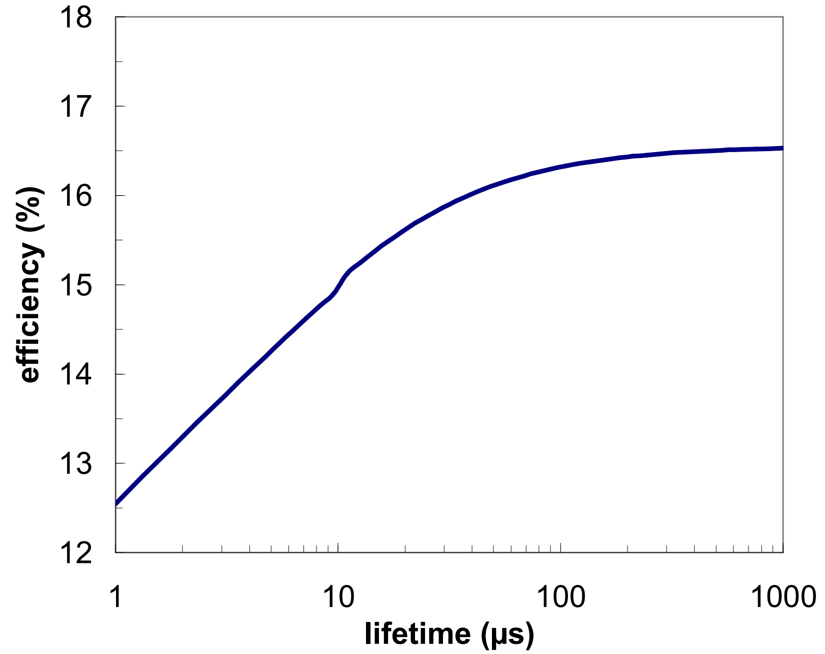
ECN

Gettering and bulk passivation (emitter and SiN_x:H)

Improved bulk quality using gettering and passivation

- Lifetime>100 μs will hardly affect cell efficiency (diffusion length 2 times cell thickness)
- Besides higher efficiency, gettering and passivation will result in a narrower efficiency distribution.





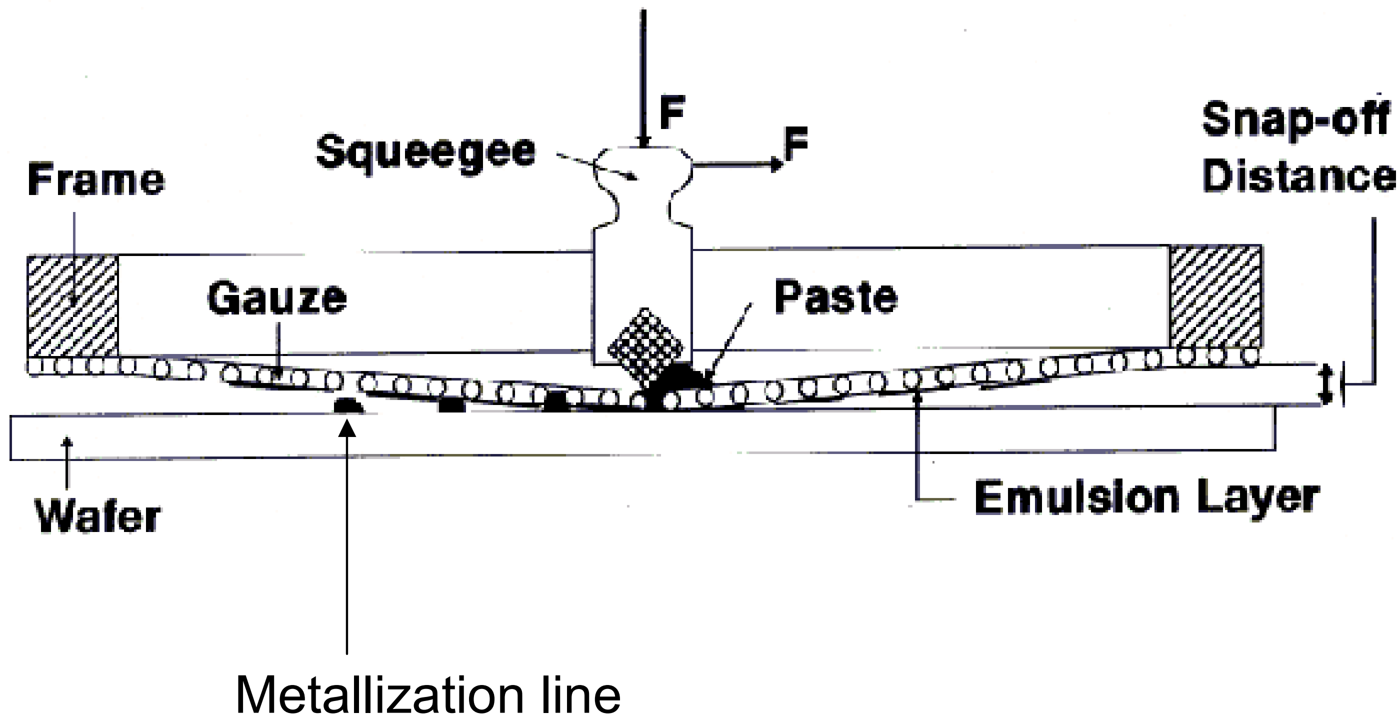
Metallization

Screen-printing process and sintering in belt furnace

Metallization

Principle screen-printing process

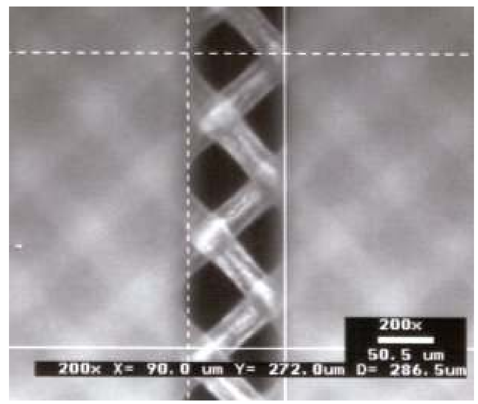
- Metallization paste is ‘pressed’ through pattern in screen
- Paste contains metal particles and oxides (etches Si at higher T)



Metallization

Ag front side metallization

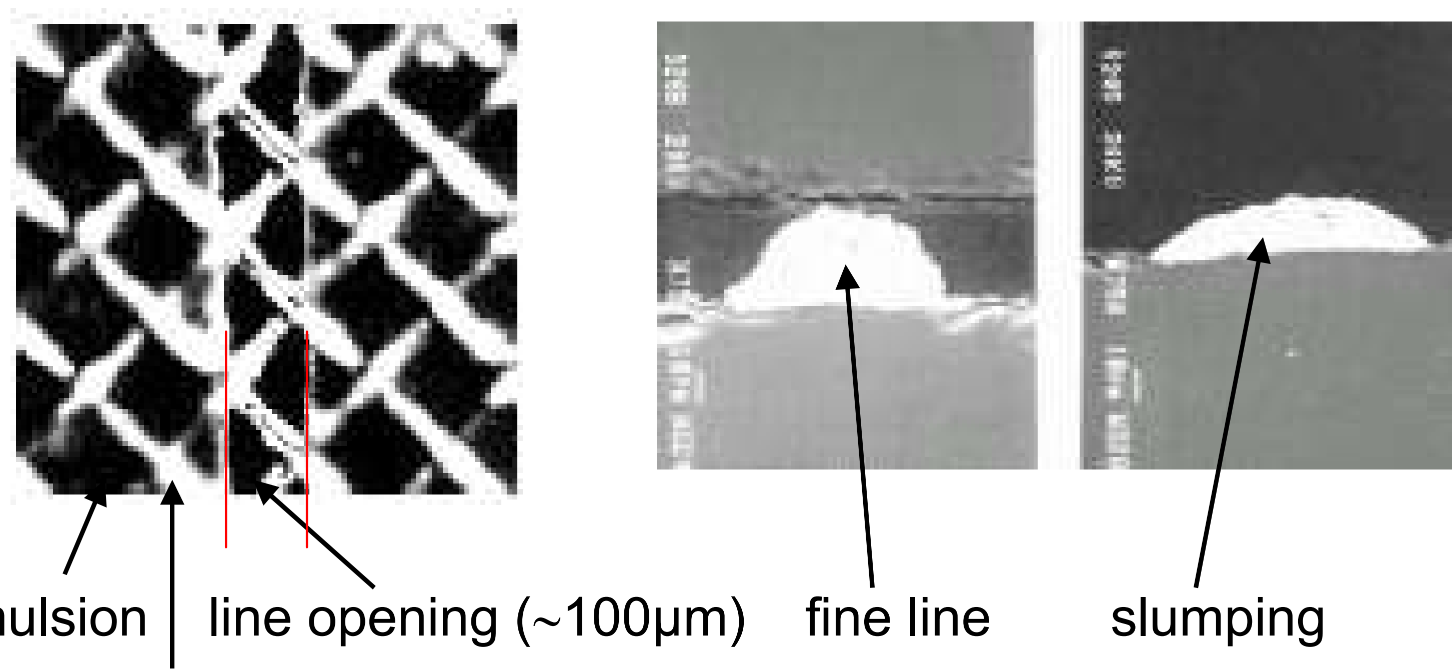
- Fine line metallization printed through patterned screen



Metallization

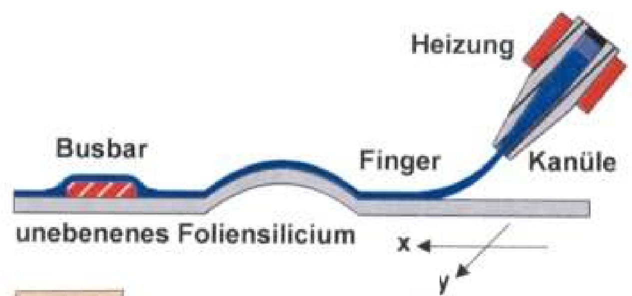
Fine line printing

- Reduced shading losses
- Contact resistance might be critical

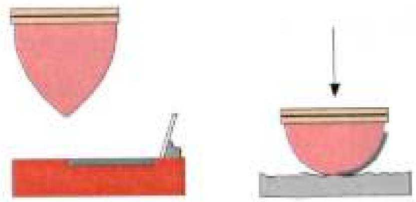


Metallization

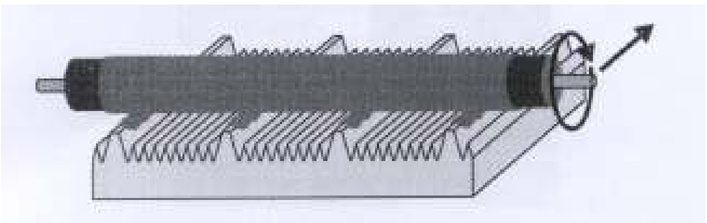
- Other techniques:
- Plating (electroless)
- Dispensing



- Pad printing



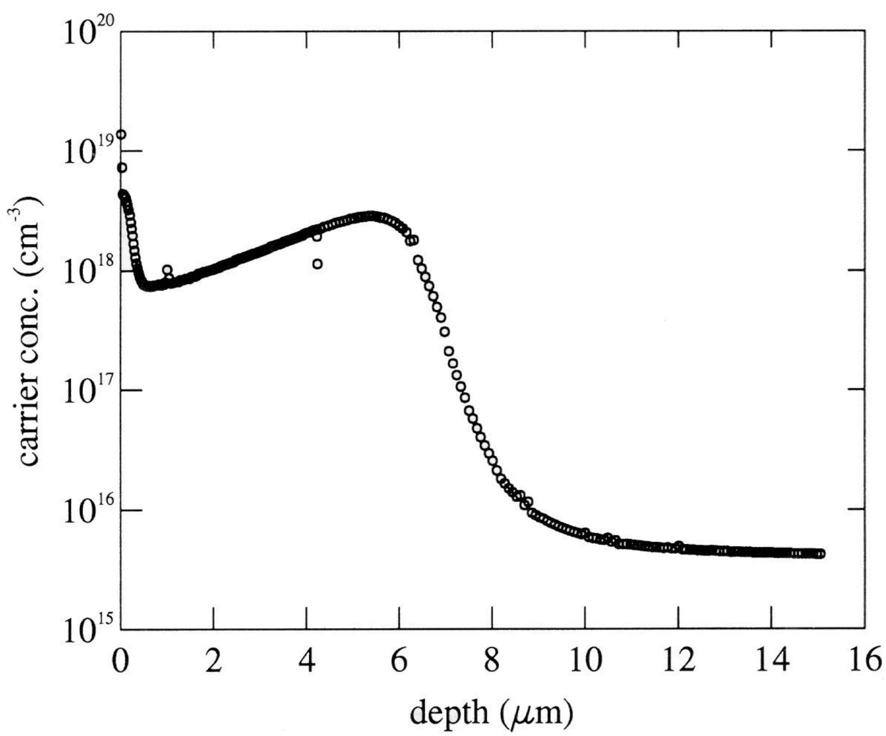
- Roller printing



Metallization

Al rear side (Back Surface Field to reduce recombination at surface)

- After sintering step (around 800 C, few seconds) highly doped layer
- Better BSF when thicker and higher doped



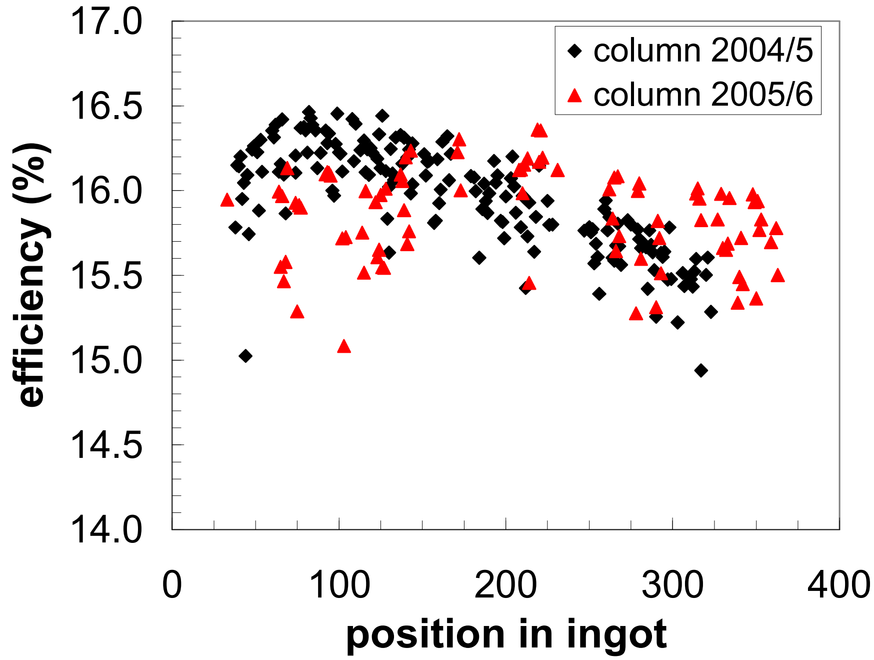
ECN

Efficiency ECN process

Results ECN Baseline process

Processing two complete columns (different ingots) of wafers during 2 years

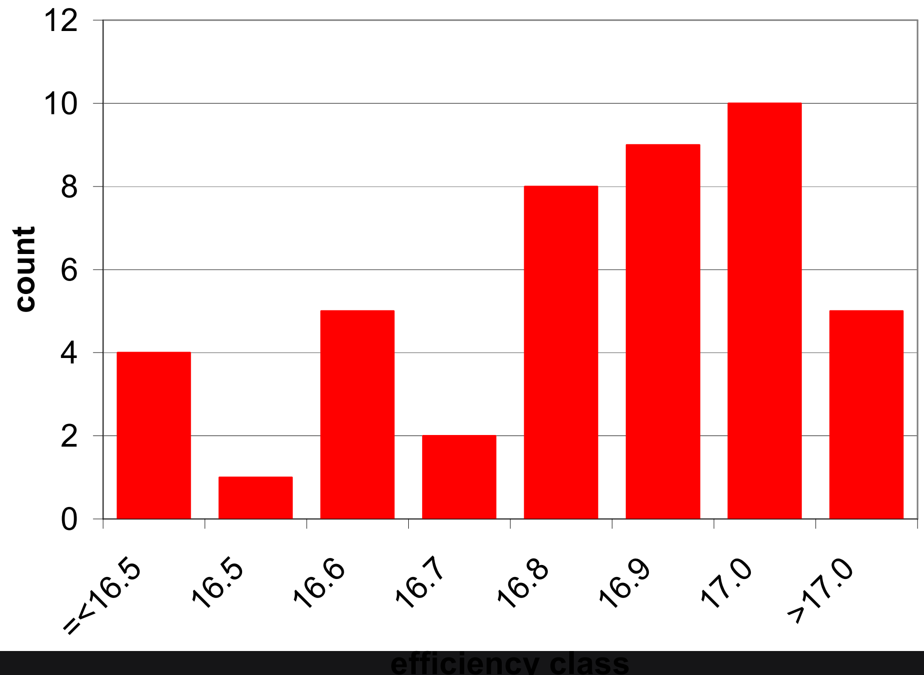
- Average 16.0% (125x125 mm^2; 300 µm thin)
- In industry about 15-16% (156x156 mm^2; 200 µm thin)



Production line with full ECN-process

Efficiency ECN process

- High-efficiency (17%) in-line process (300 µm thick; 156 cm^2 mc-Si)
  - 50 cells processed (best efficiency 17.1%; average 16.8%)
  - Module made using cover glass with ARC
    Full area efficiency 14.8%; encapsulated cell eff: 16.8%



V_{OC}=22.2 V;
I_{SC}=5.76A;
FF=0.738;
P=94.3 Wp

ECN

Future improvements

Thin wafers

- Rear side critical

Minority carrier density

- Combination of generation and recombination

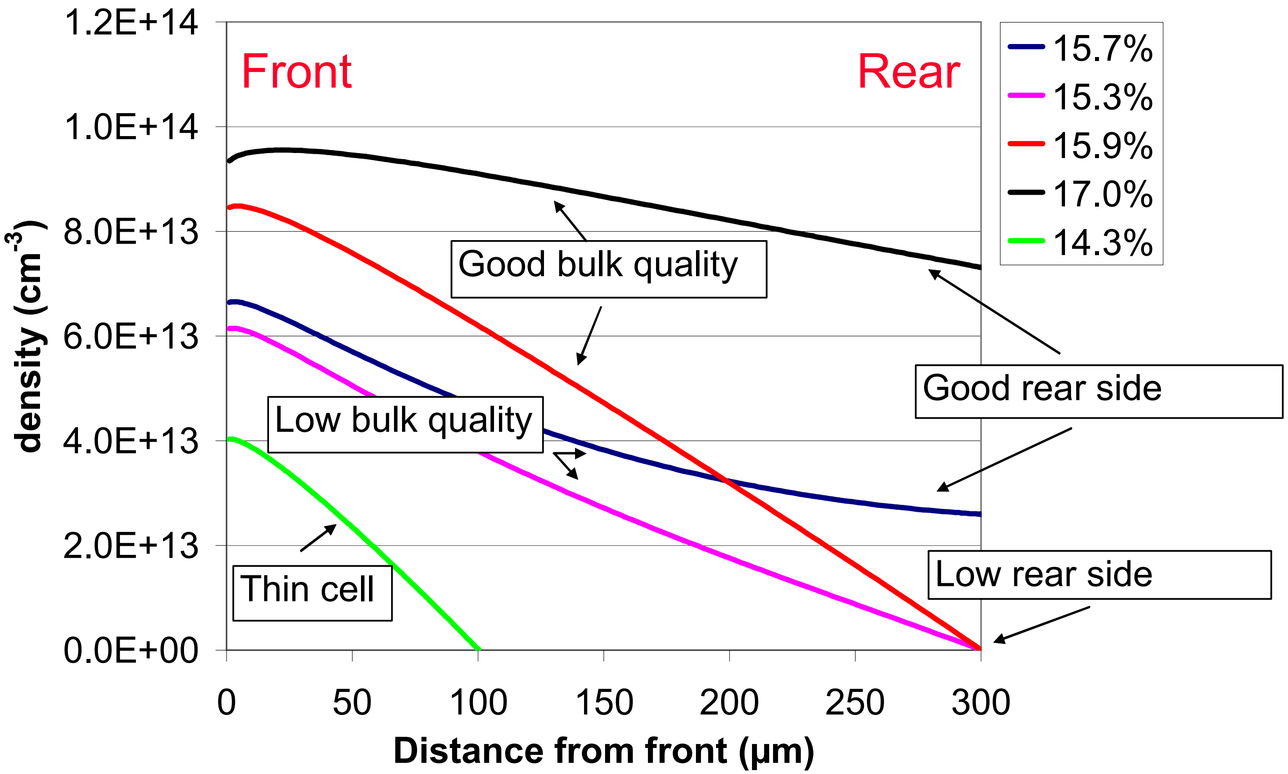
17.0%: good bulk and rear

15.9%: good bulk, low rear

15.7%: low bulk, good rear

15.3%: low bulk and rear

14.3%: as 15.9%, but thin



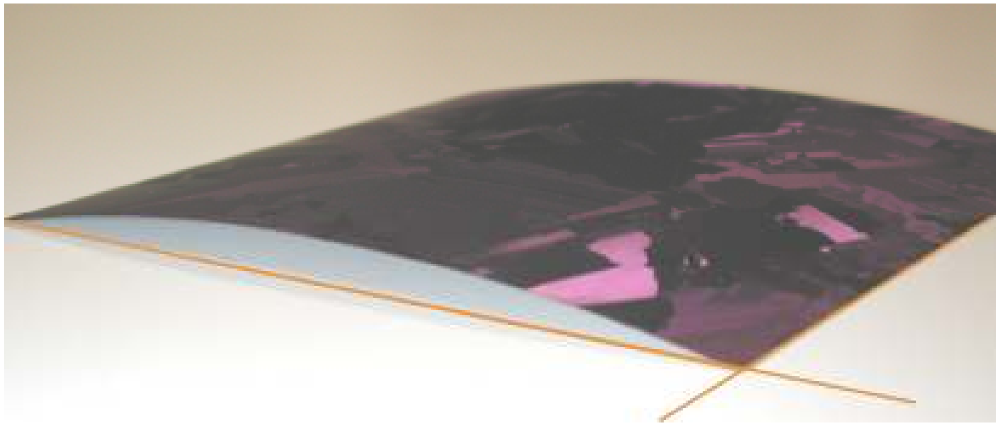
Future improvement

Al rear side (Back Surface Field to reduce recombination at surface)

- 17% reached on 300 µm thick wafers

However:

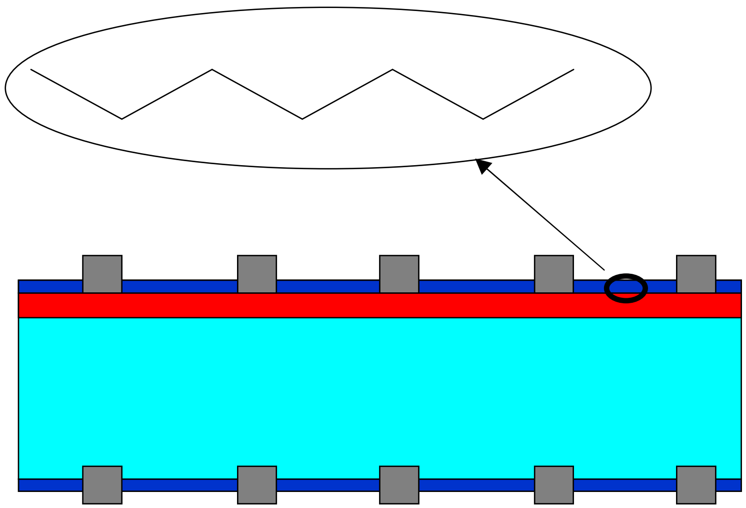
- Bowing for thinner wafers
- Recombination losses too high for high efficiencies (>18%)
- Internal reflection too low (~70%) for high efficiencies



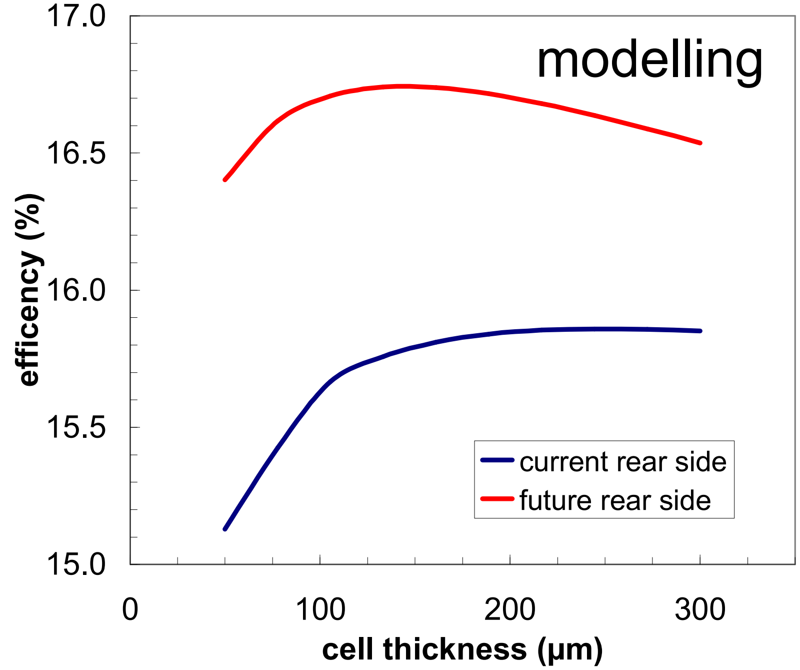
Future improvements rear side

Thin wafers

- Rear side critical (bowing, reflection, BSF)
- New rear side processing using for example SiN_x
  - Higher efficiencies for thinner wafers



SiN_x for rear side passivation
Local rear contacts / BSF



Future improvements rear side

Thin wafers

- New rear side processing using SiN_x
  - 16.4% obtained by ECN with baseline-like processing
  - About 1% absolute higher than reference with Al BSF (obtained efficiency depends on Si material quality)

ECN

Future improvements

Thin wafers (less dependent on material quality)

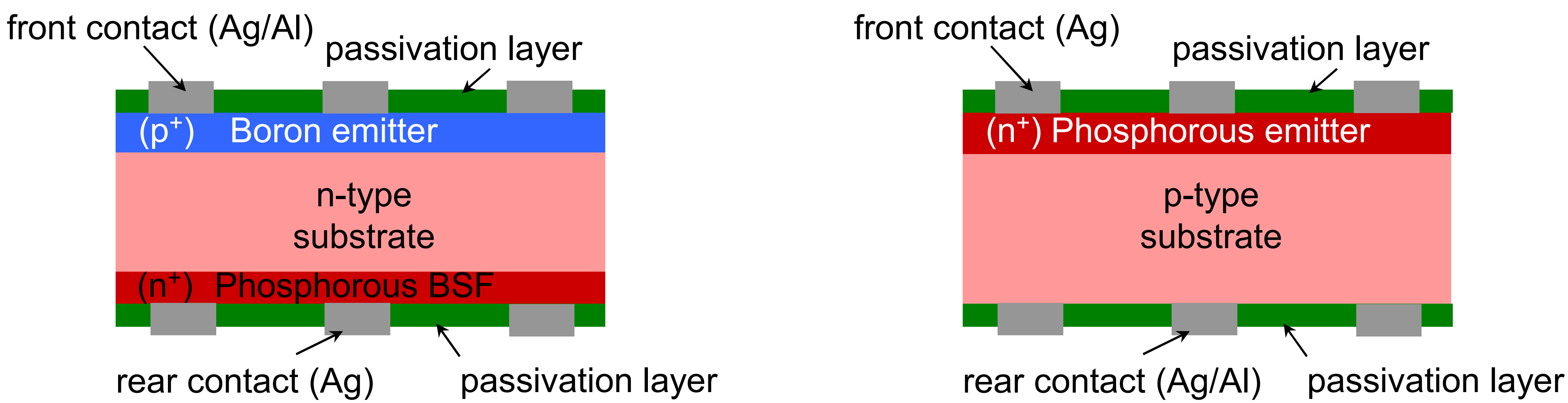
- Improved light management
  - Texturing
  - Light trapping
- Improved emitter (reduce losses)
- Perfect surface passivation
  - Both surfaces
- Less metallization losses
  - Series resistance (contact and line resistance)
  - Reduced shading losses

20% mc-Si cell efficiency should be possible! (long term)

Future improvements

Thin wafers (less dependent on material quality)

- n-type material
  - More tolerant for most impurities
  - 16.7% on mc-Si
  - 18.5% on Cz Si^{confirmed}

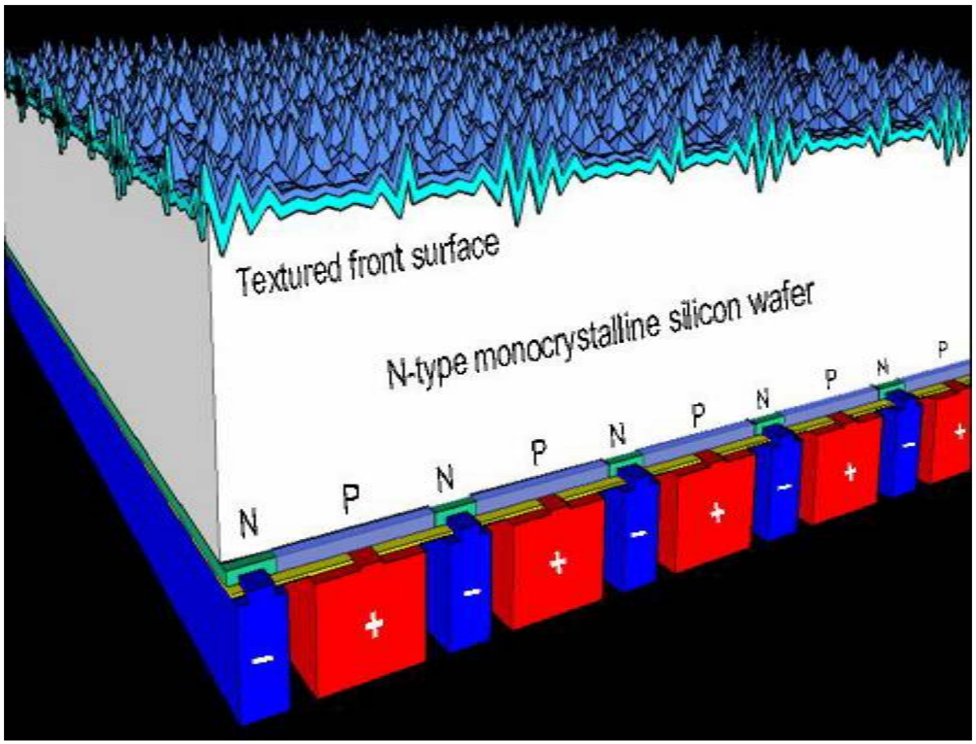


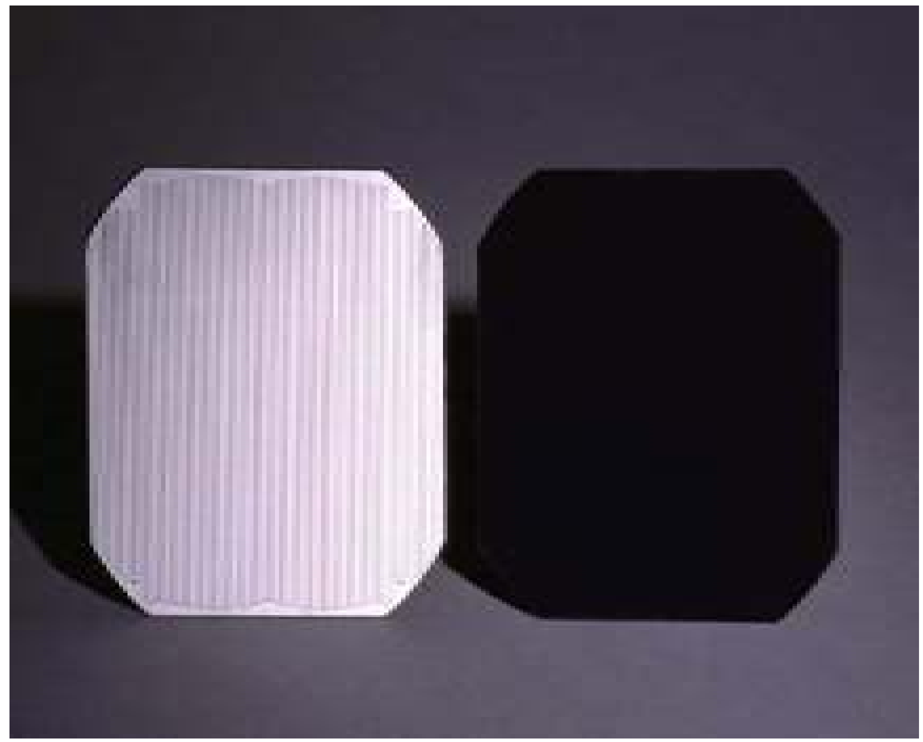
20% mc-Si cell efficiency should be possible! (long term)

Other industrial cell concepts

Rear side contacted cell

SunPower: 22.4% average!

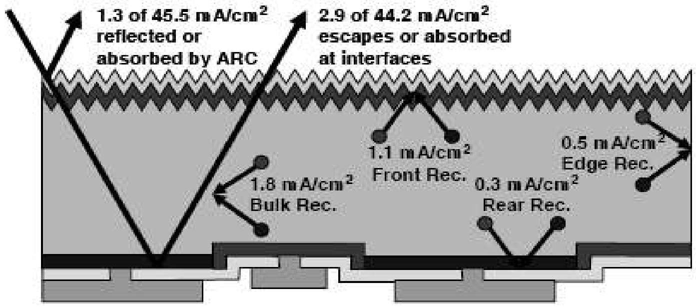


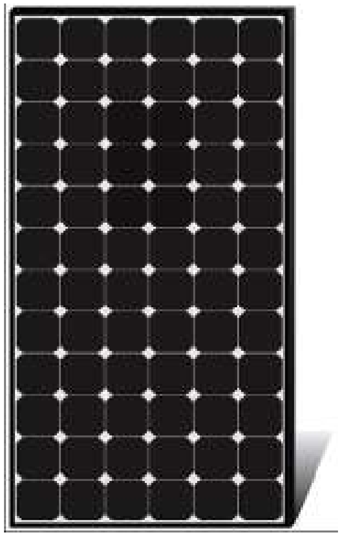


Other industrial cell concepts

SunPower

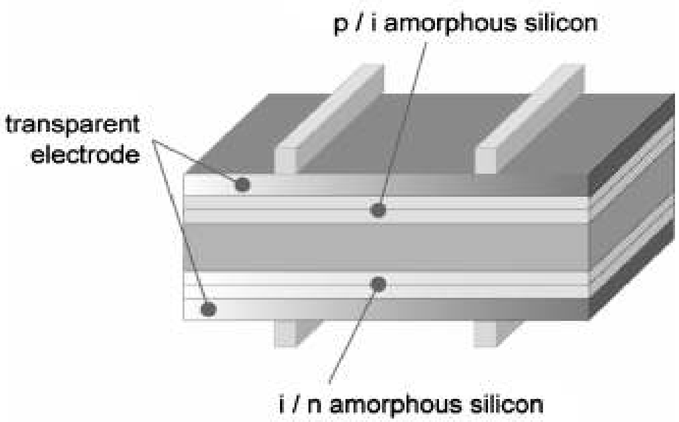
- Cell 23.4%
- n-type material
- Module: full area 20.1%





Sanyo

- HIT cell: 22.3%
- n-type material
- Emitter deposited

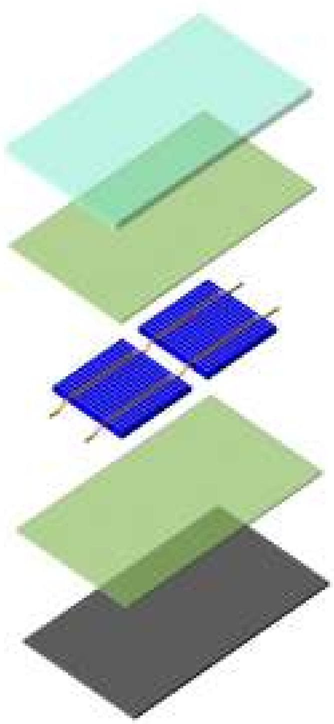


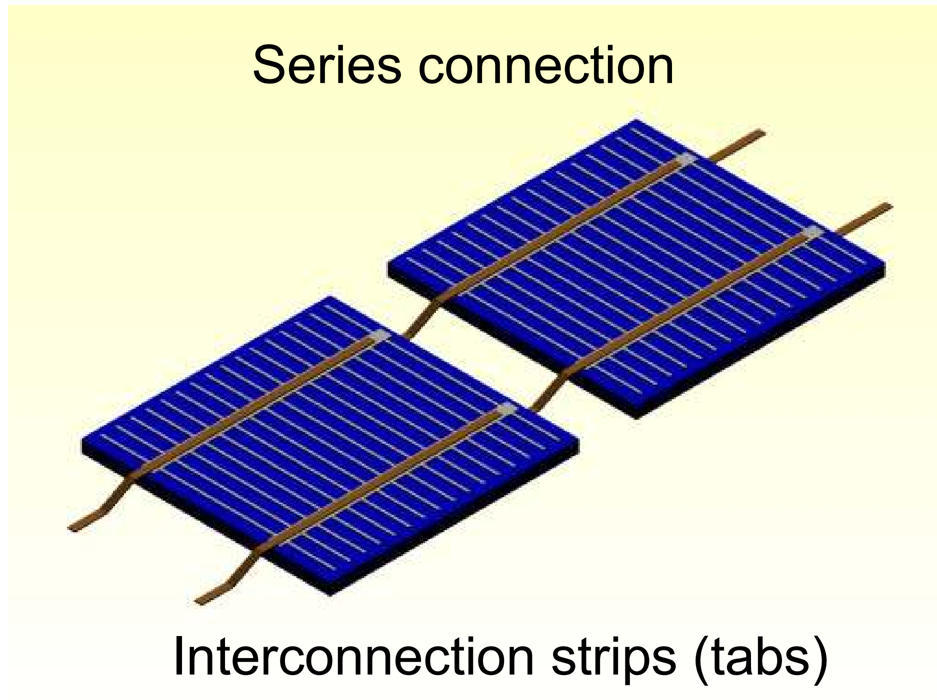
Record efficiencies (independently confirmed)

Monocrystalline (4 cm^2):	25.0%
Monocrystalline (FZ, 147 cm^2):	22.0%
Monycrystalline (Cz, 100 cm^2):	22.5%
Multicrystalline (1 cm^2):	20.4%
Multicrystalline (217 cm^2):	18.7%
ECN multi (243 cm^2):	17.4%

Module technology

Conventional module technology (soldering)





Module technology

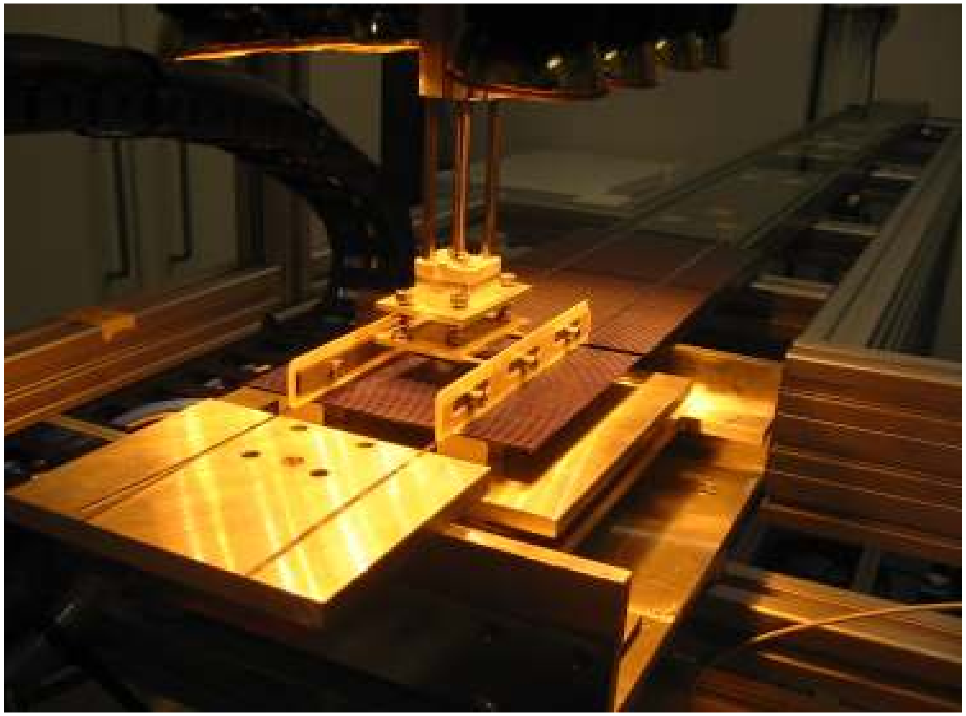
Conventional module technology

interconnection

lamination

Module technology

Pilot-line tabber-stringer for interconnection

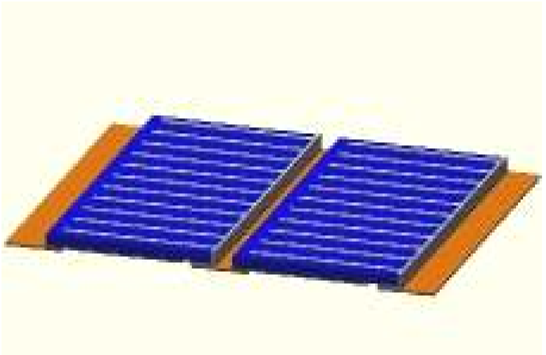


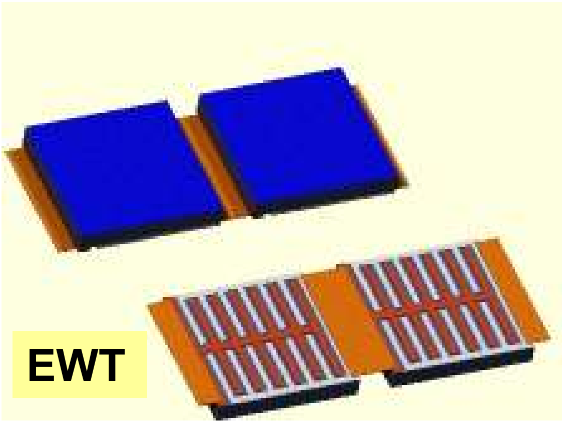
Module technology

New module technology:

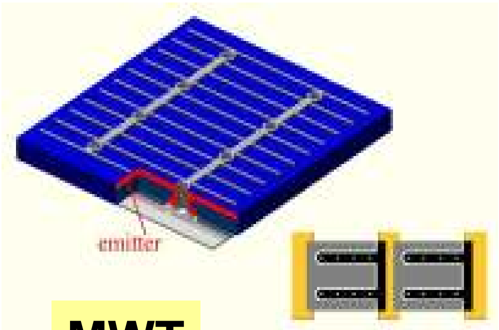
- New cell designs needed
  - Back contacted
  - Simple interconnection
  - Can be used for thin cells

MWA

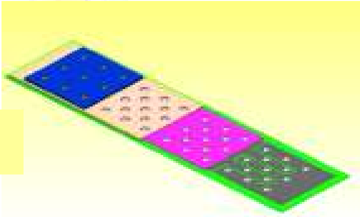




EWT



MWT

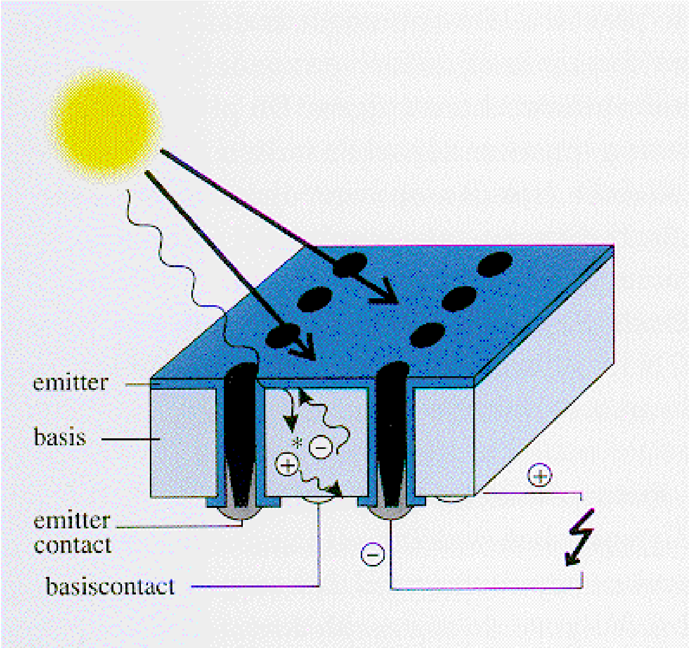


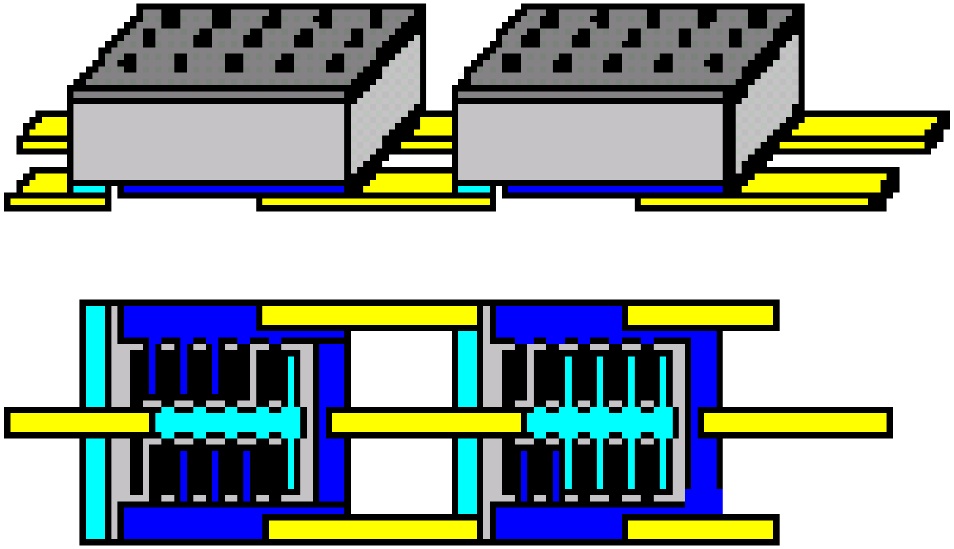
PUM

Module technology

Emitter Wrap Through:

- No metallization on the front
- Thousands of holes

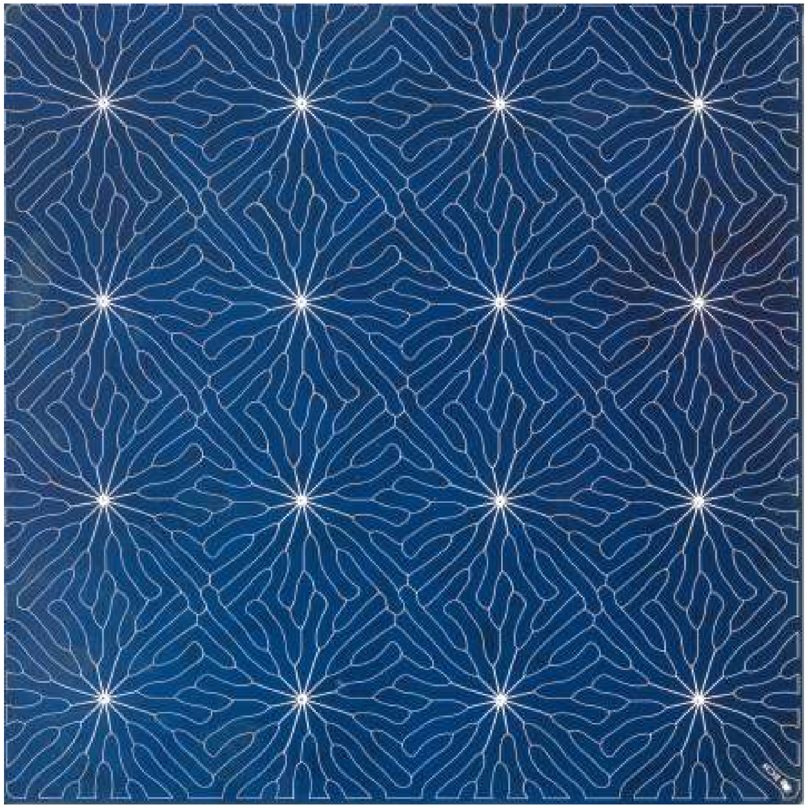




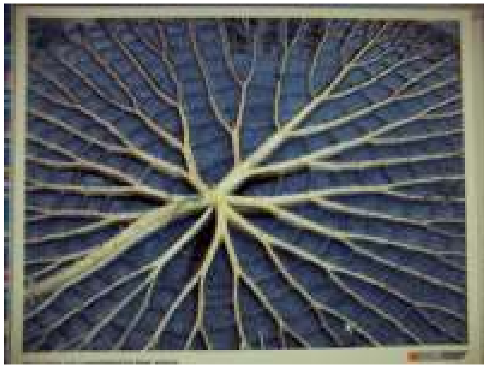
Module technology

ECN's PUM concept:

- More energy from attractive cells
- 2-3% less shading
- Resistance losses independent on cell size (only on size unit cell)
- Standard cell processing except:
  - Laser drilling holes
  - Junction isolation around holes



Mother Nature's water lily

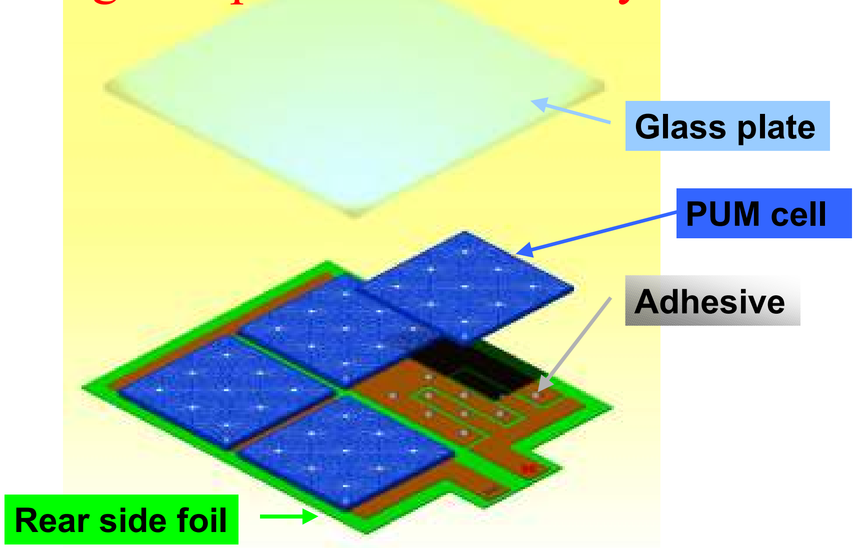


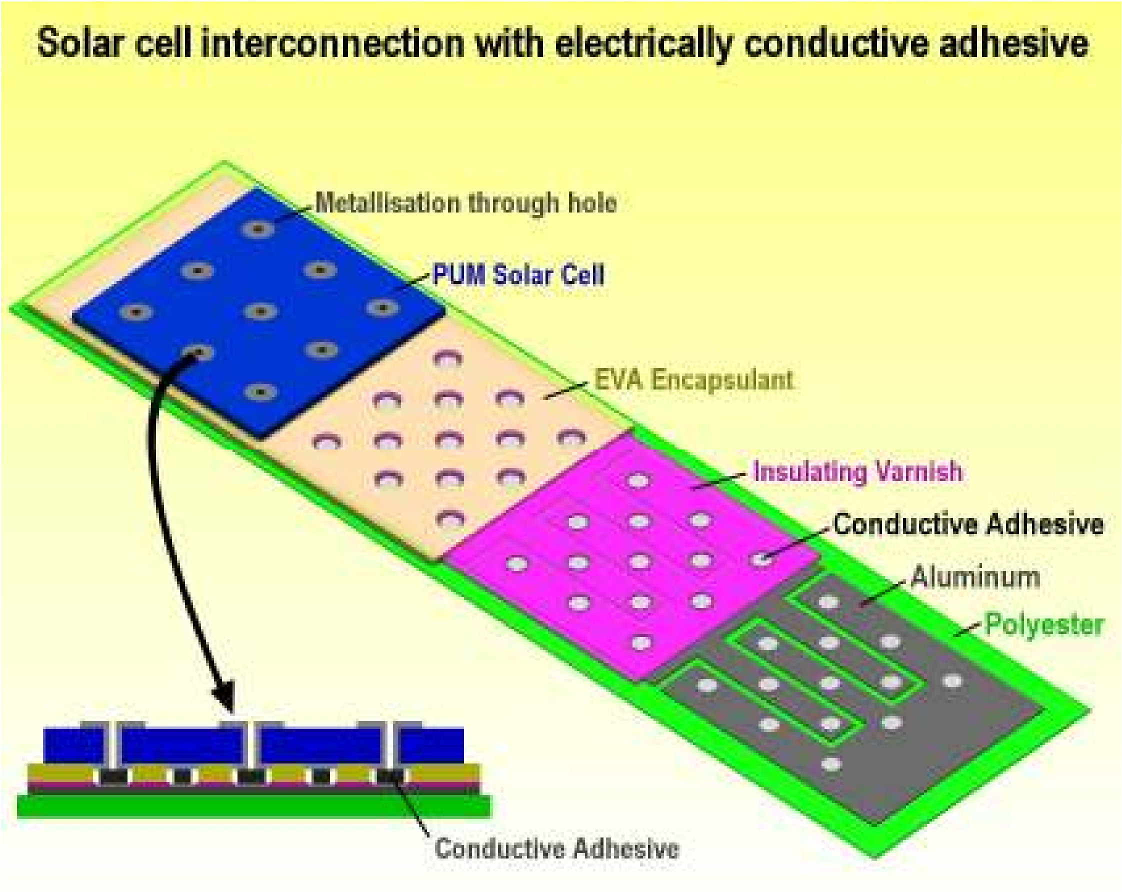
Module technology

ECN's PUM concept:

- Single shot interconnection and encapsulation

Single step module assembly

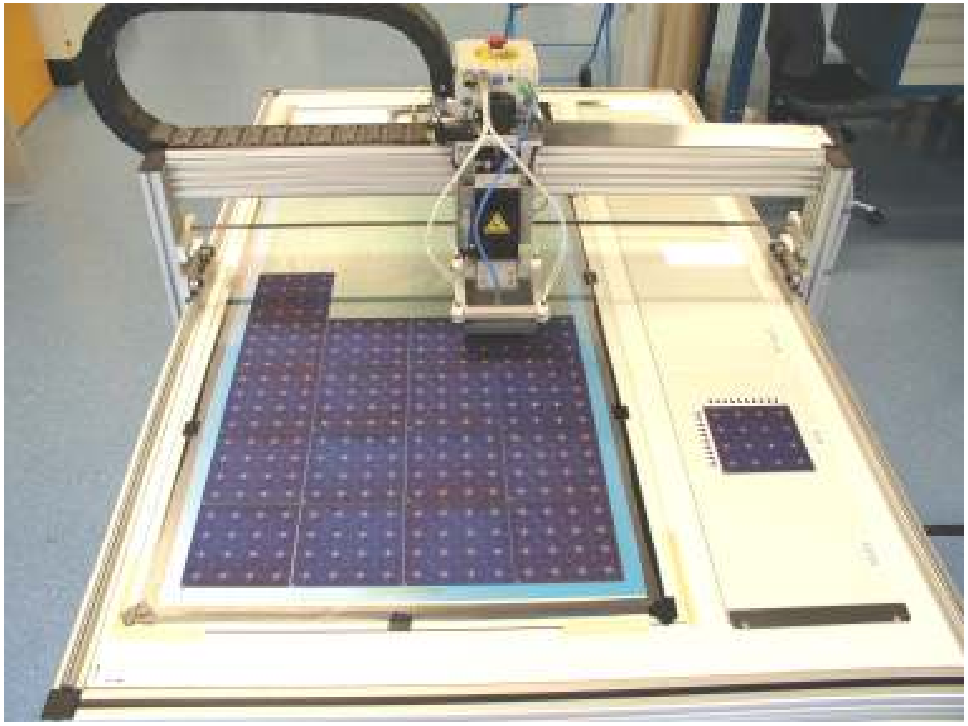




Module technology

ECN's PUM process:

- Foil preparation
- Apply conductive adhesive instead of soldering (lower stress)
- Pick and place cells
- One step curing and encapsulation



Module technology

ECN's PUM result:

- Full size module
- 16.4% aperture area
  - WORLD RECORD!!

Best PUM cell result up to now:

- 17.4% (243 cm^2; 160 μm thin)
- ~80 cells: average 17.2%

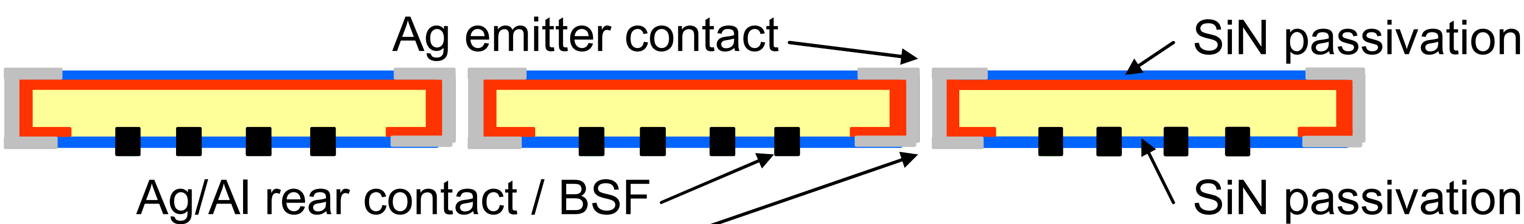
At this moment PUM is the only integrated concept for cell and module

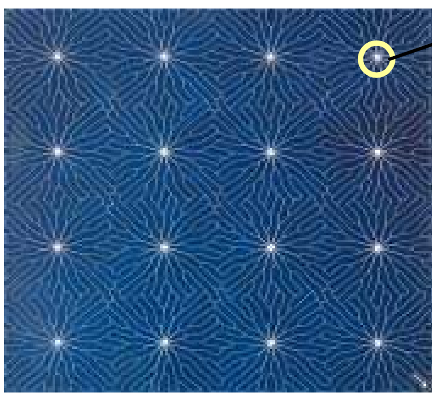
Module technology

ECN's improved PUM: ASPIRe

All Sides Passivated and Interconnected at the Rear

- 16.4% on 243 cm^2 mc-Si, 160 μm thin





Front

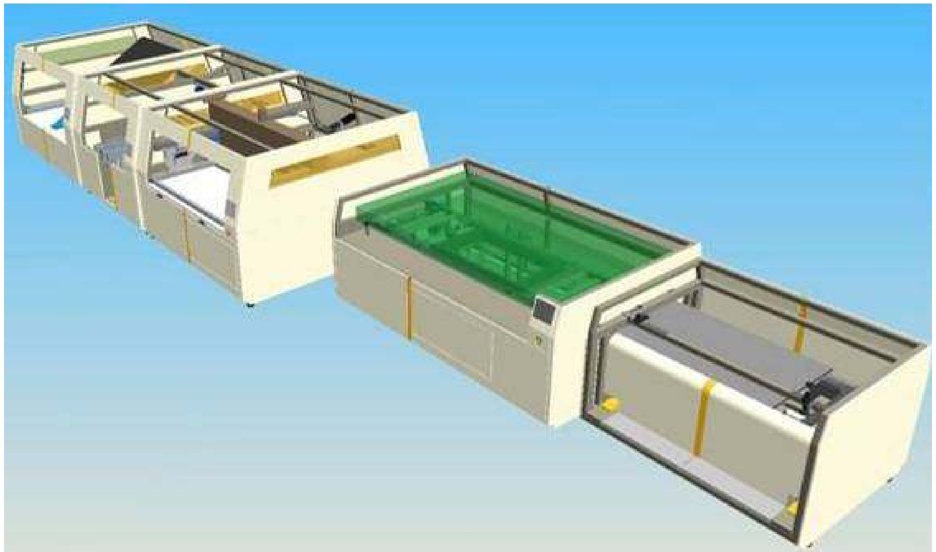
Rear

Metallization pattern courtesy of Solland Solar BV

Module technology

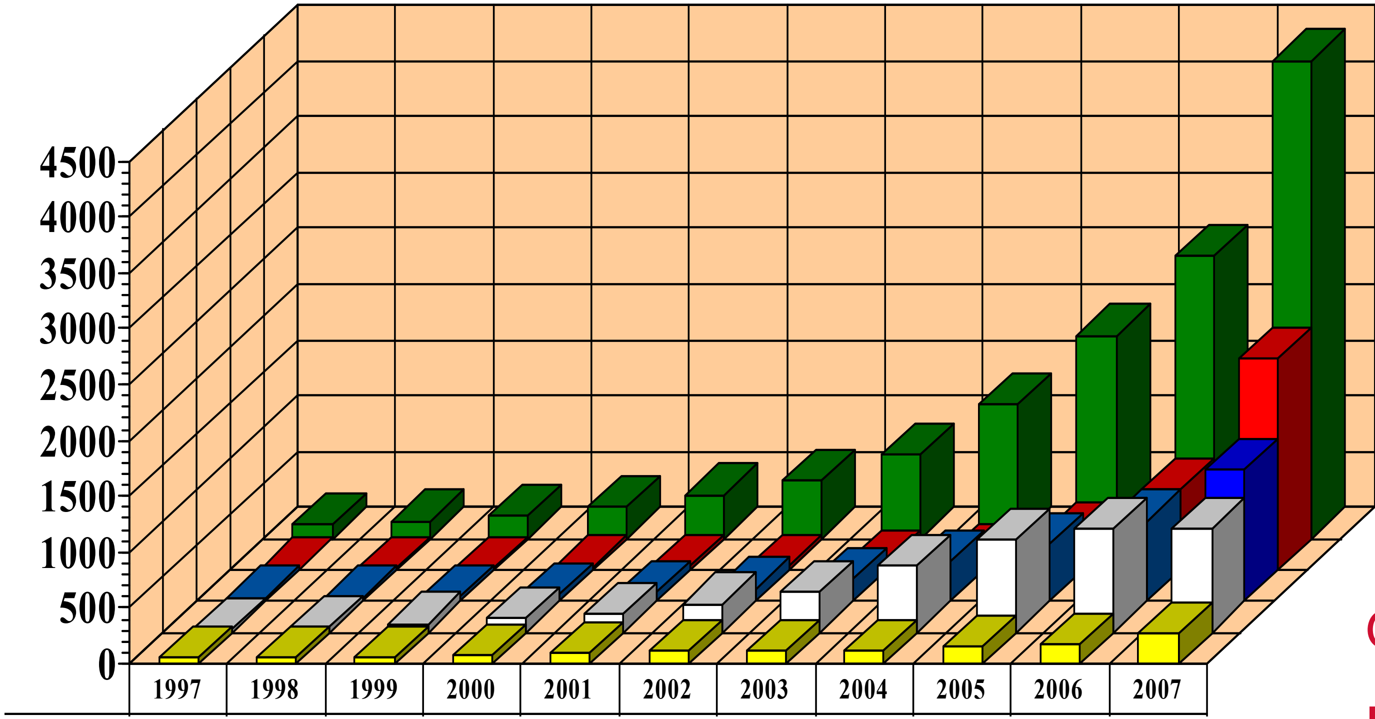
Pilot line at ECN

Fully automated process for back-contact cells and suitable for thin and fragile cells



PV market

Annual market growth: average more than 40%



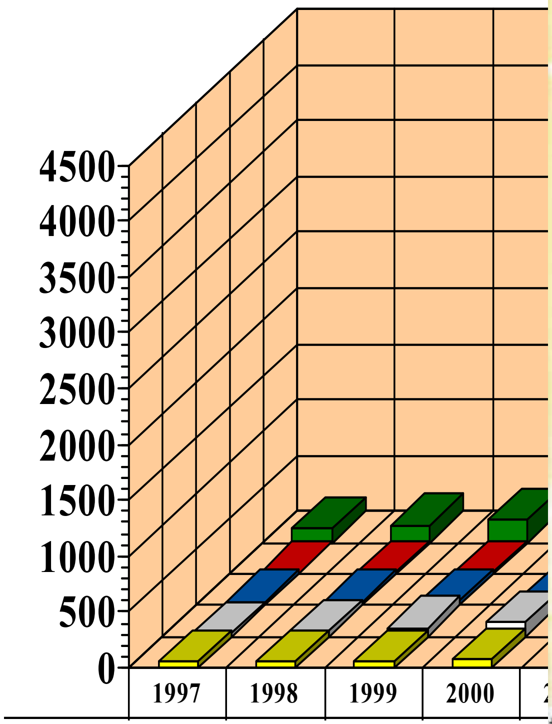
Growth rate 2007: ~70%

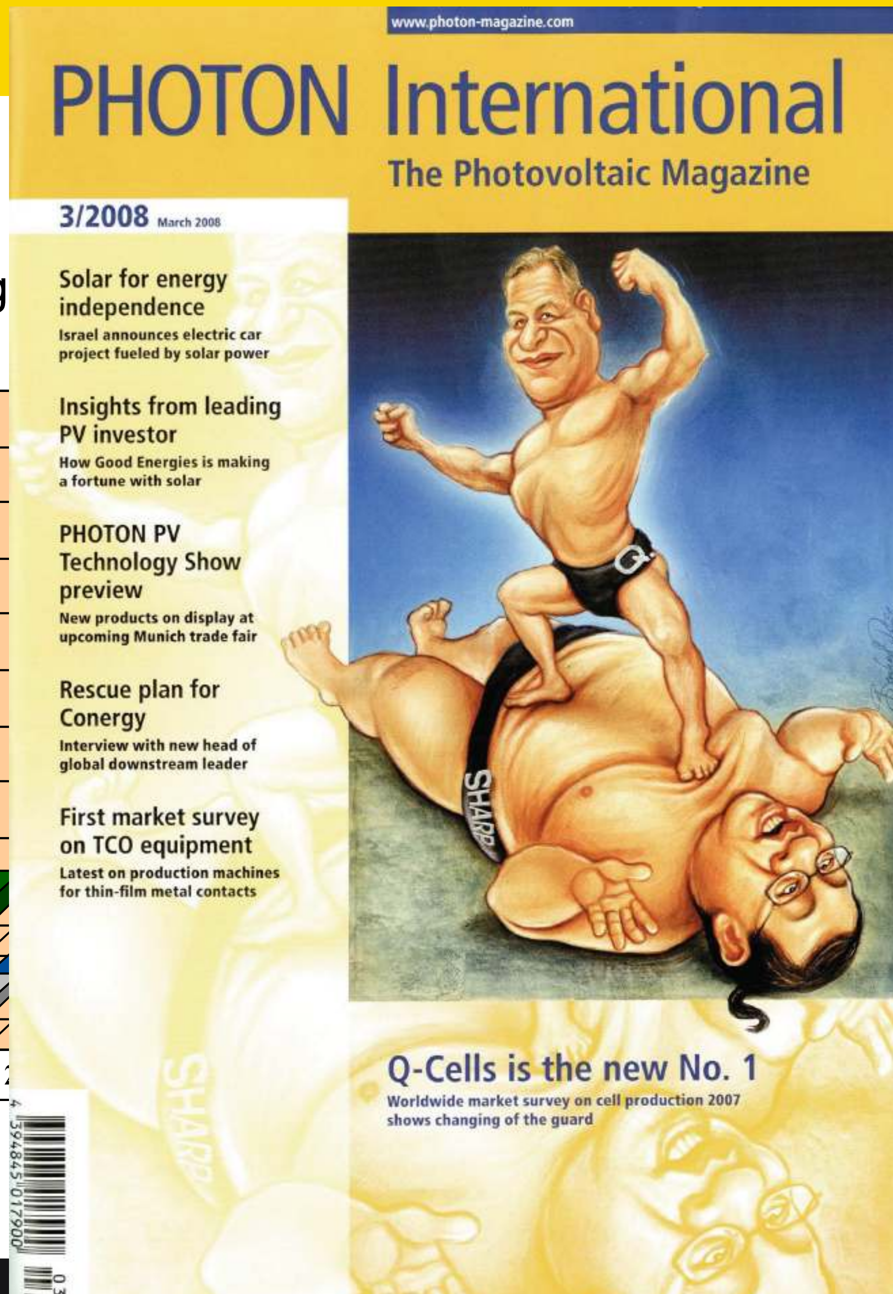
In 2007: 4.3 GWp

Photon International, 2008

PV market

Annual market g





owth rate 2007: ~70%

2007: 4.3 GWp

Photon International, 2008

PV market

~90% crystalline Si technology

mono-Si

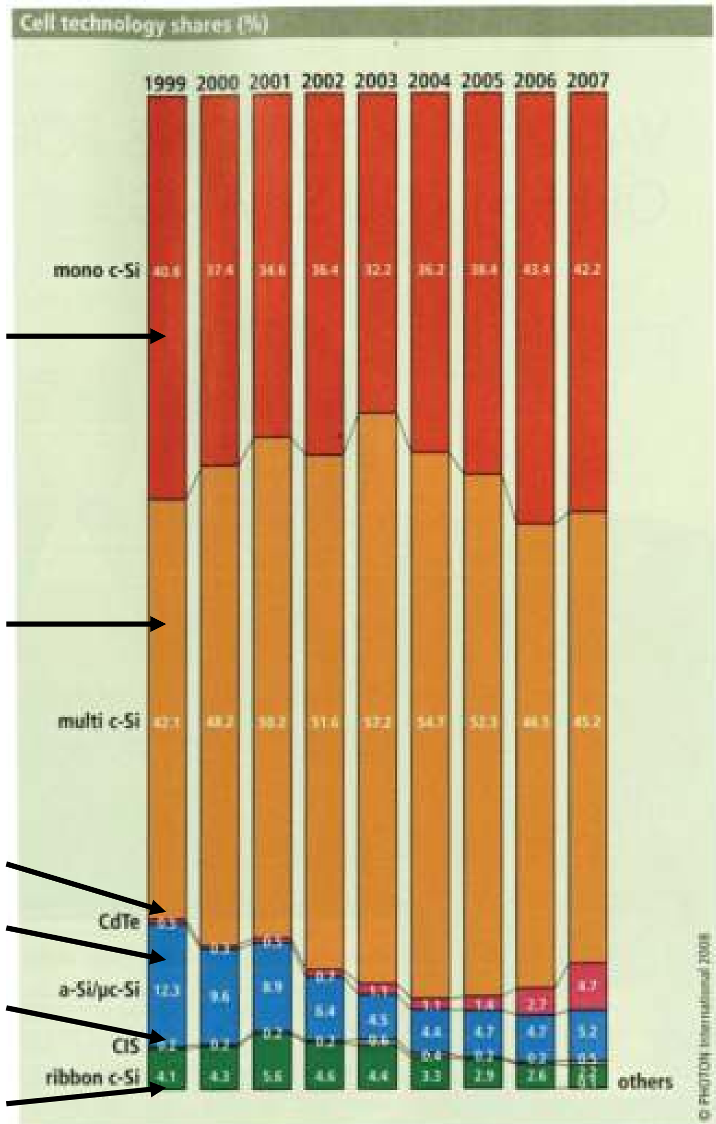
multi-Si

CdTe

Thin film Si

CIS

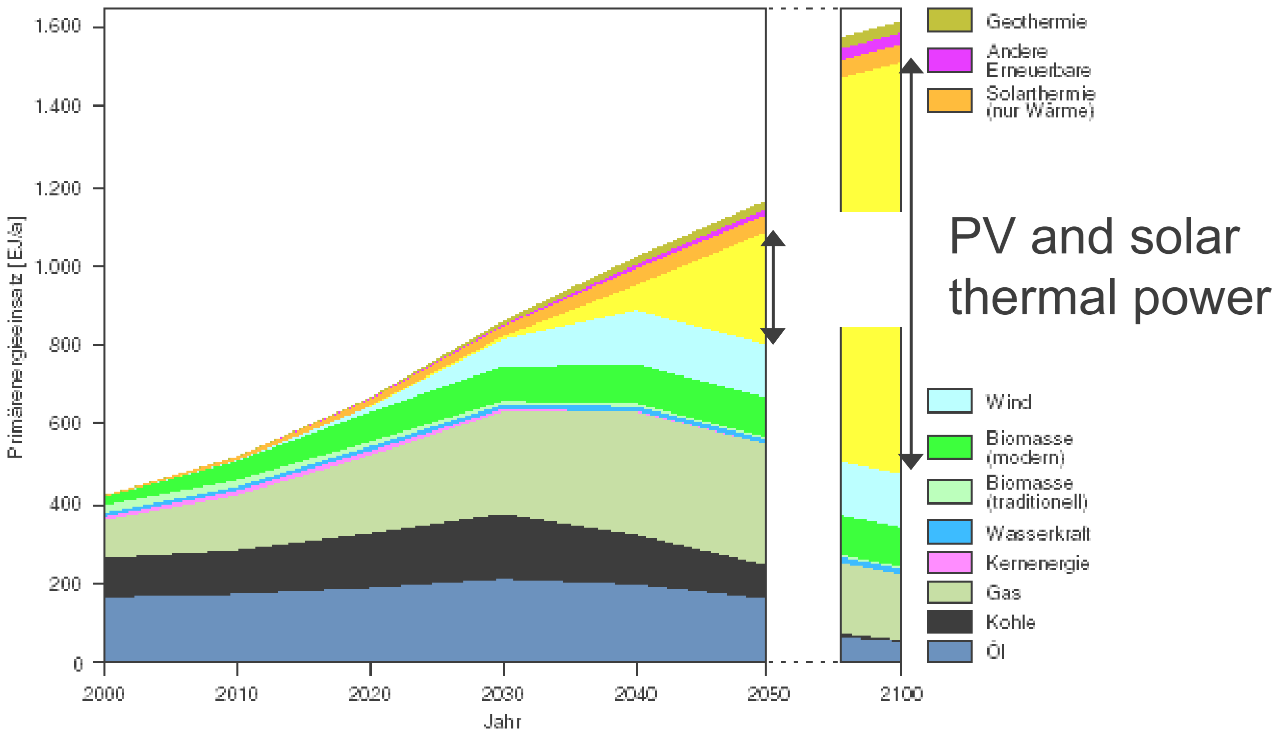
Ribbon Si



Photon International, 2008

PV market

Expected market: solar the most important primary energy source



Wissenschaftliche Beirat 2003

Costs PV

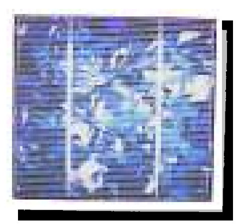
Contributes wafer is about 45%!

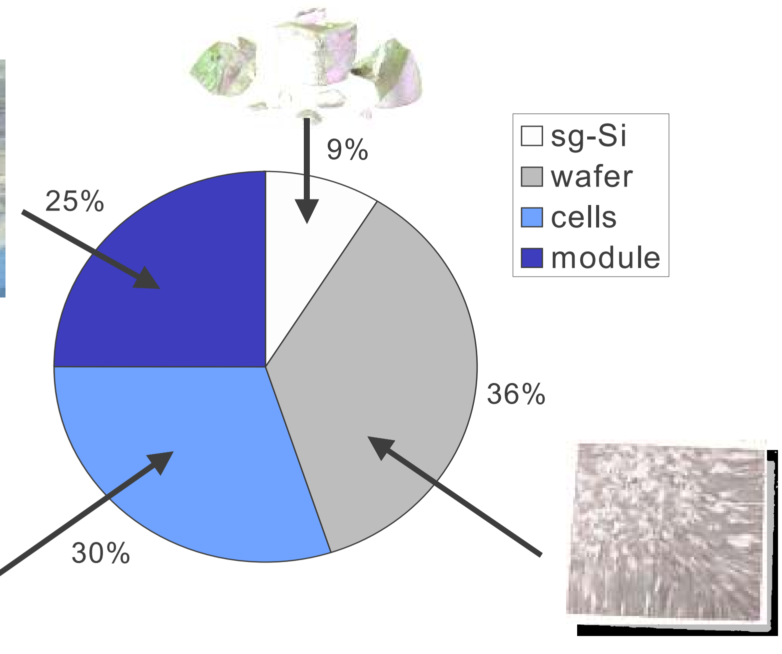
Thinner wafers, or better ribbons, important!

Price solar electricity:

0.20-0.50 €/kWh
(depending on location)

NL: ~0.50 €/kWh





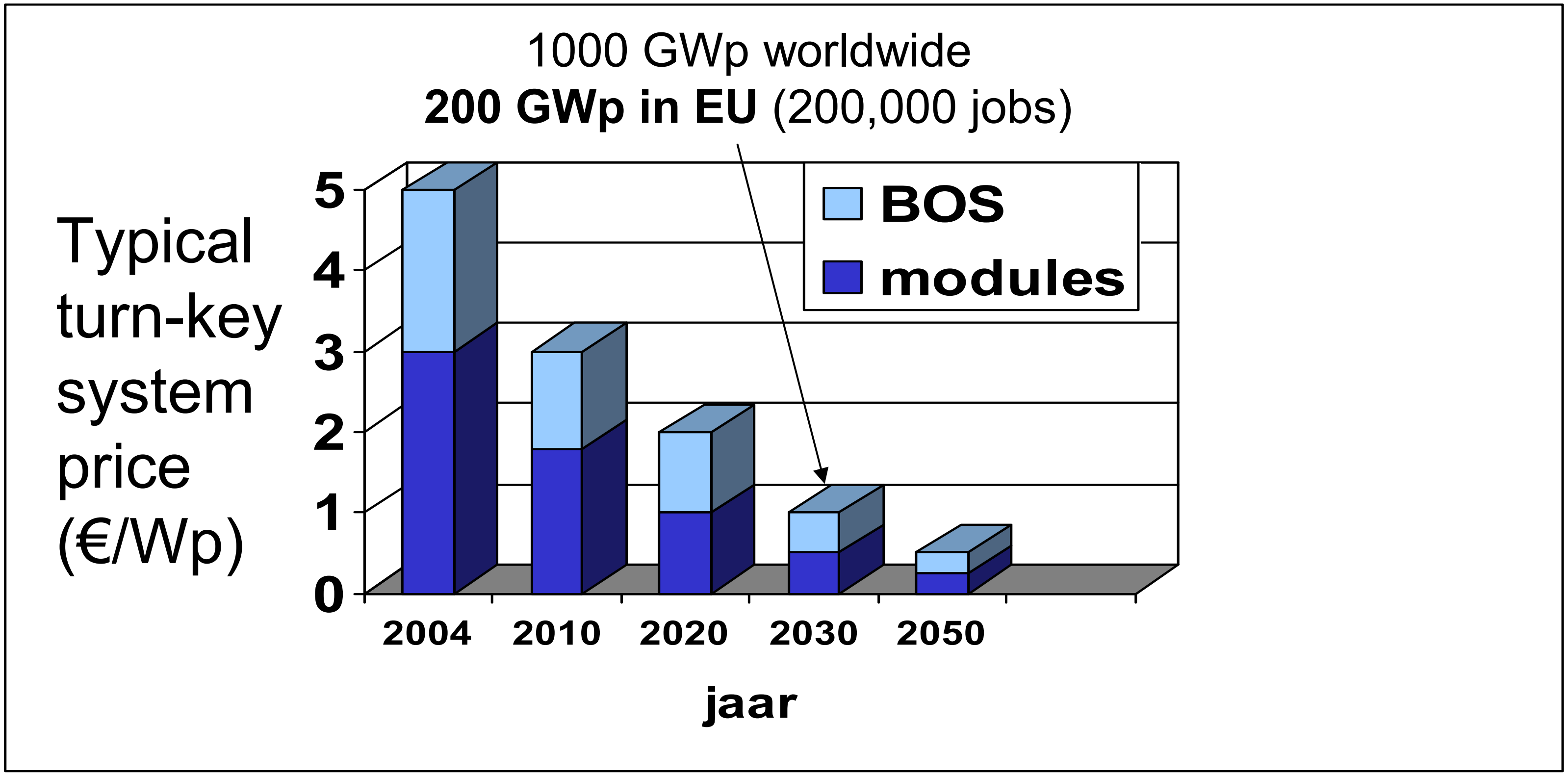
Cost reduction PV

- Less material use
  - Thin ribbons
  - Less module materials
- High efficiencies for the same process costs
  - Advanced processing
  - New cell design
- Easy manufacturing
  - Automation
  - Easy module manufacturing
- High lifetime
- Improved yearly system output

ECN

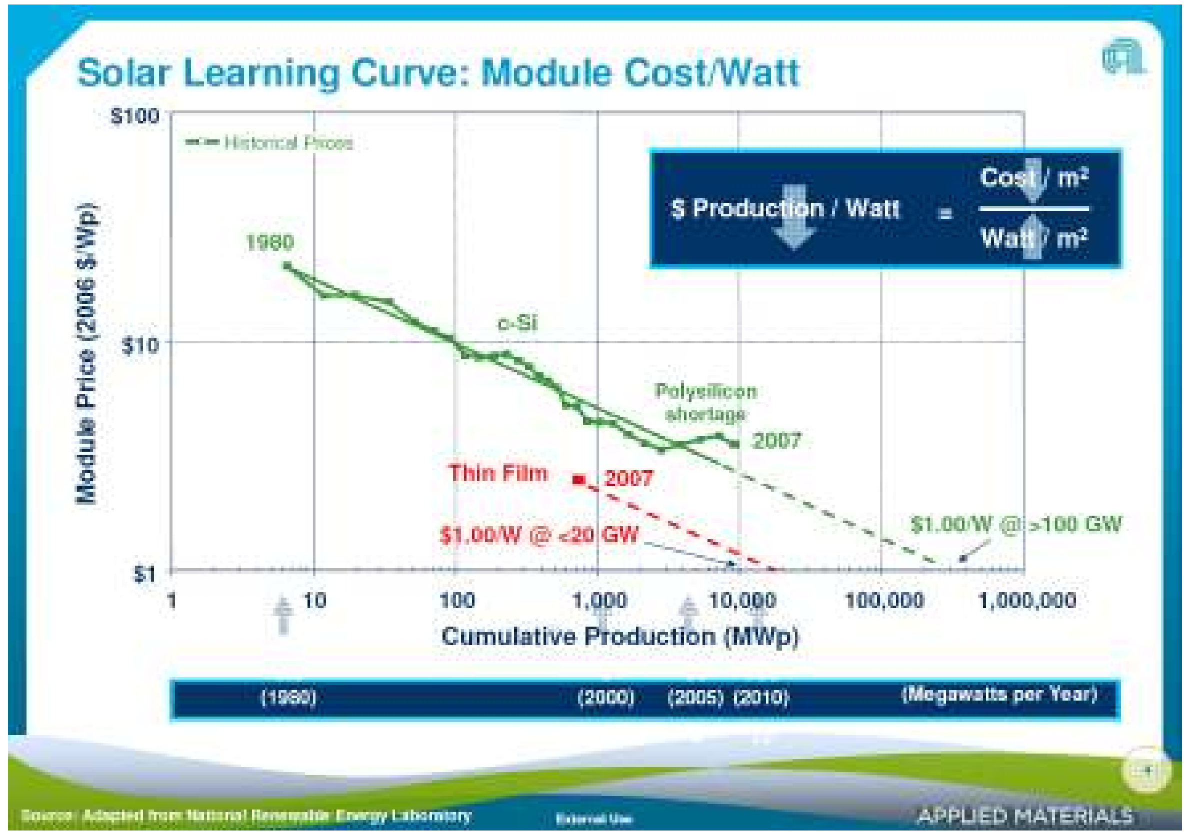
Cost reduction PV

- Expected costs



Cost reduction PV

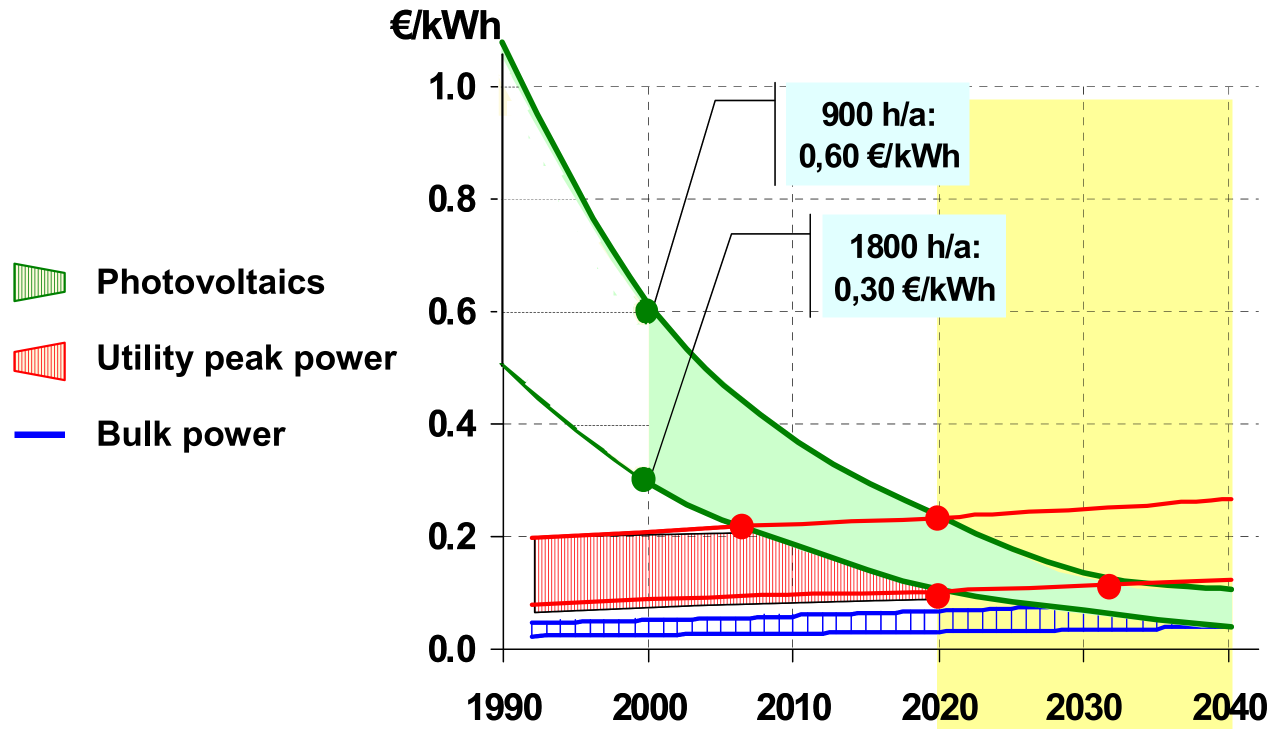
- Expected costs based on learning curves (EU project Photex)
  - Combined effect of technology development, experience, ….
  - Progress ratio PR should be around 80%



Cost reduction PV

- Expected costs

- Solar competitive between 2010-2020

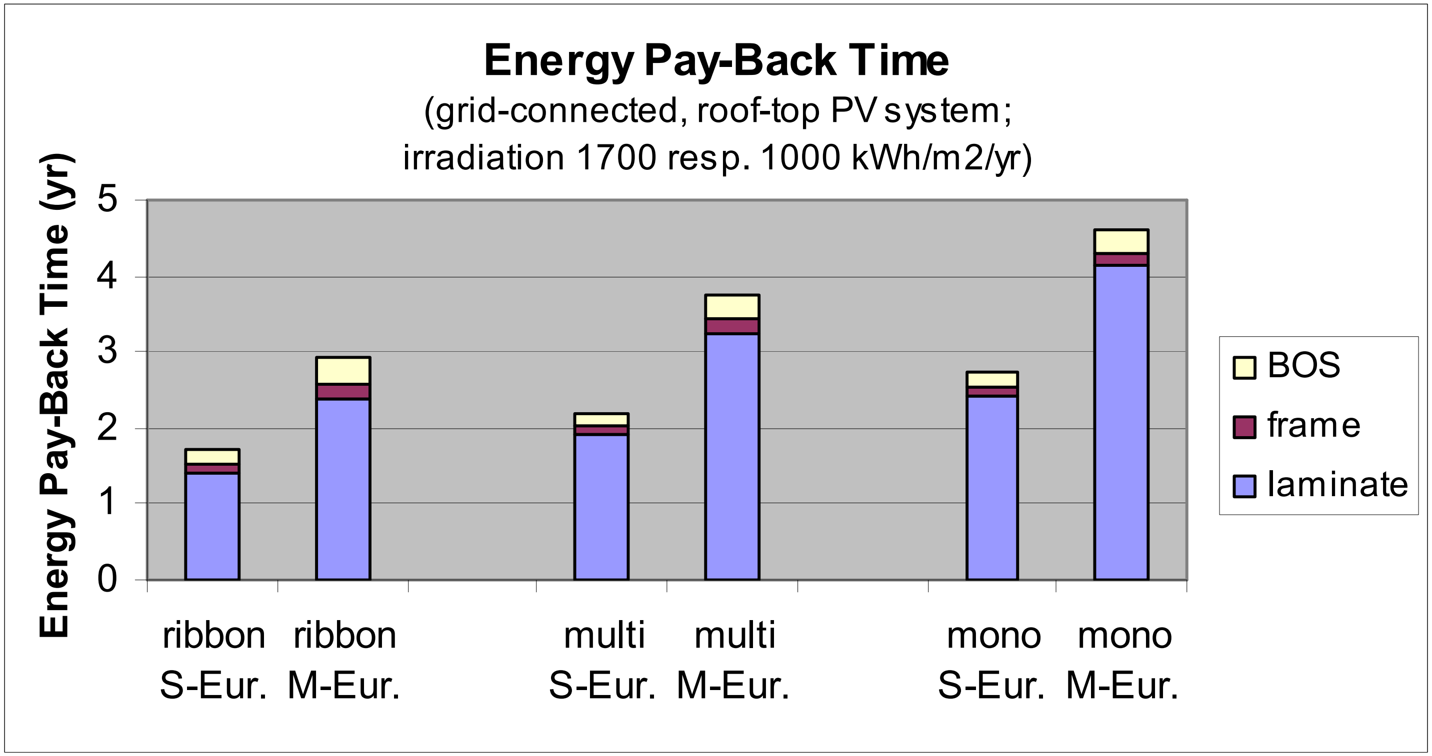


Source: RWE Energie AG and RSS GmbH

Towards an Effective European Industrial Policy for PV.ppt / 05.06.2004 / Rapp @ RWE SCHOTT Solar GmbH

Environmental aspects

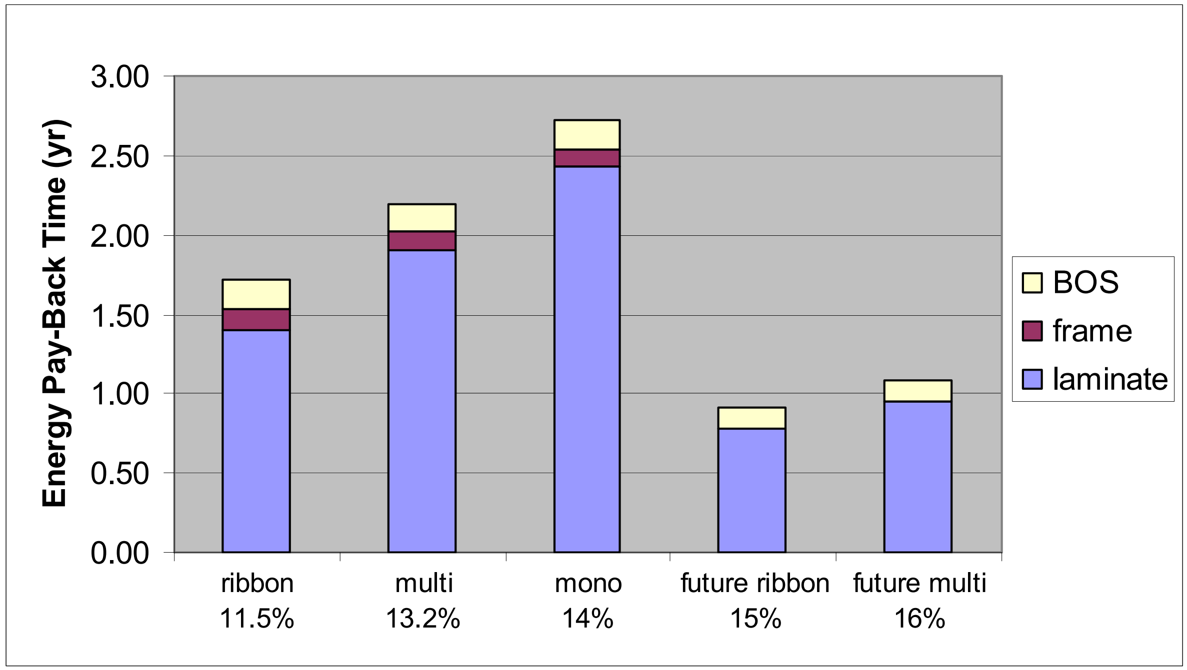
- Energy Pay Back Time 2005



Environmental aspects

Energy Pay Back Time 2005 and 2010+

- Low energy consumption especially for Solar Grade Si
- Low material use (abundance)
- High efficiency
- High lifetime modules
- Environmental friendly processes
- Recycling



Conclusions

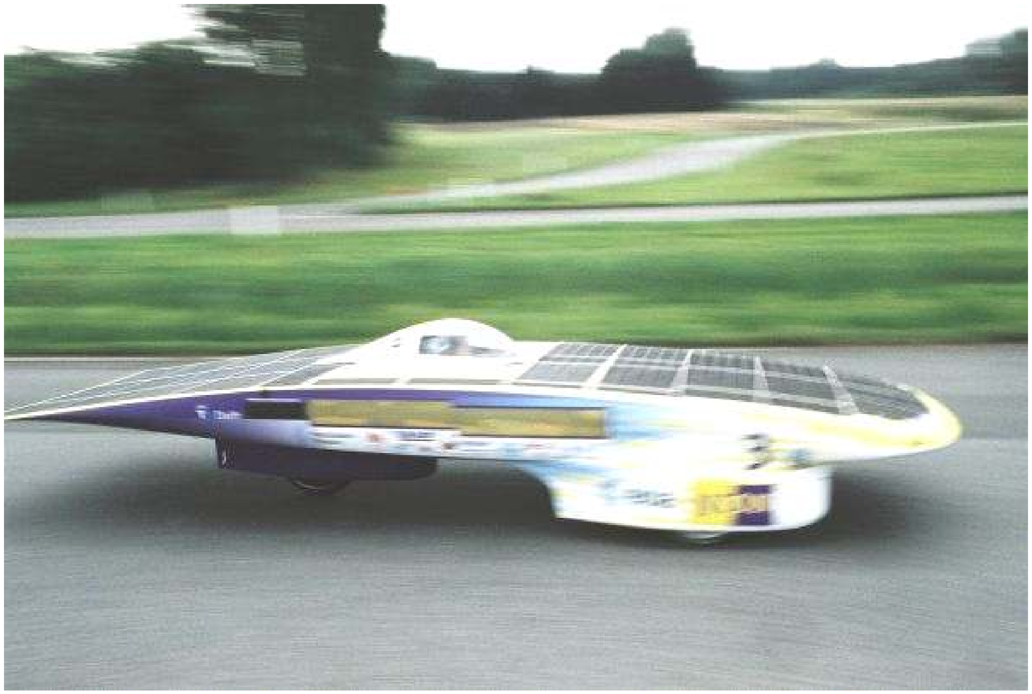
- Solar Grade Silicon needed for growing market
  - Effect of impurities on cell efficiency should be known
- Less Si use with ribbons
- Improved processing has led to 17% mc-Si efficiency using in-line processing
- New processes for thin wafers/ribbons under development
- Integrated cell and module design like PUM needed
- High module lifetime

Then

- Cost reduction possible
  - Will be competitive with bulk electricity price
- Energy Pay Back Time can be reduced to <1 year
- Solar energy will be the most important primary energy source in 2100

Applications at ECN

Applications




Thank you for your kind attention
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